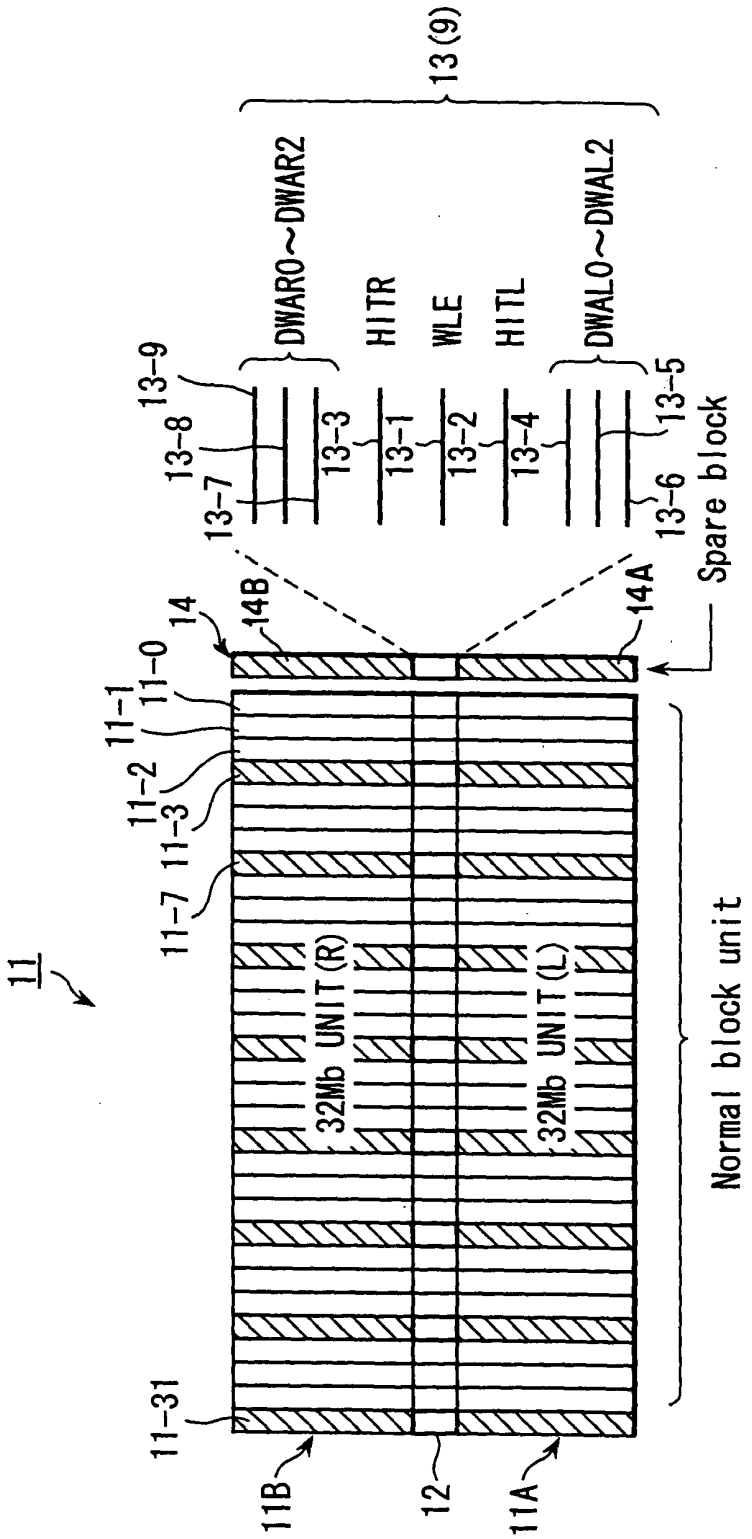

11
11-31
11-7
11-3
11-2
11-1
11-0
14
14B
14A
13(9)
DWAR0~DWAR2
HITR
WLE
HITL
DWAL0~DWAL2
13-9
13-8
13-7
13-3
13-1
13-2
13-4
13-6
13-5
Spare block
Normal block unit
32Mb UNIT(R)
32Mb UNIT(L)
11B
12
11A

FIG. 1

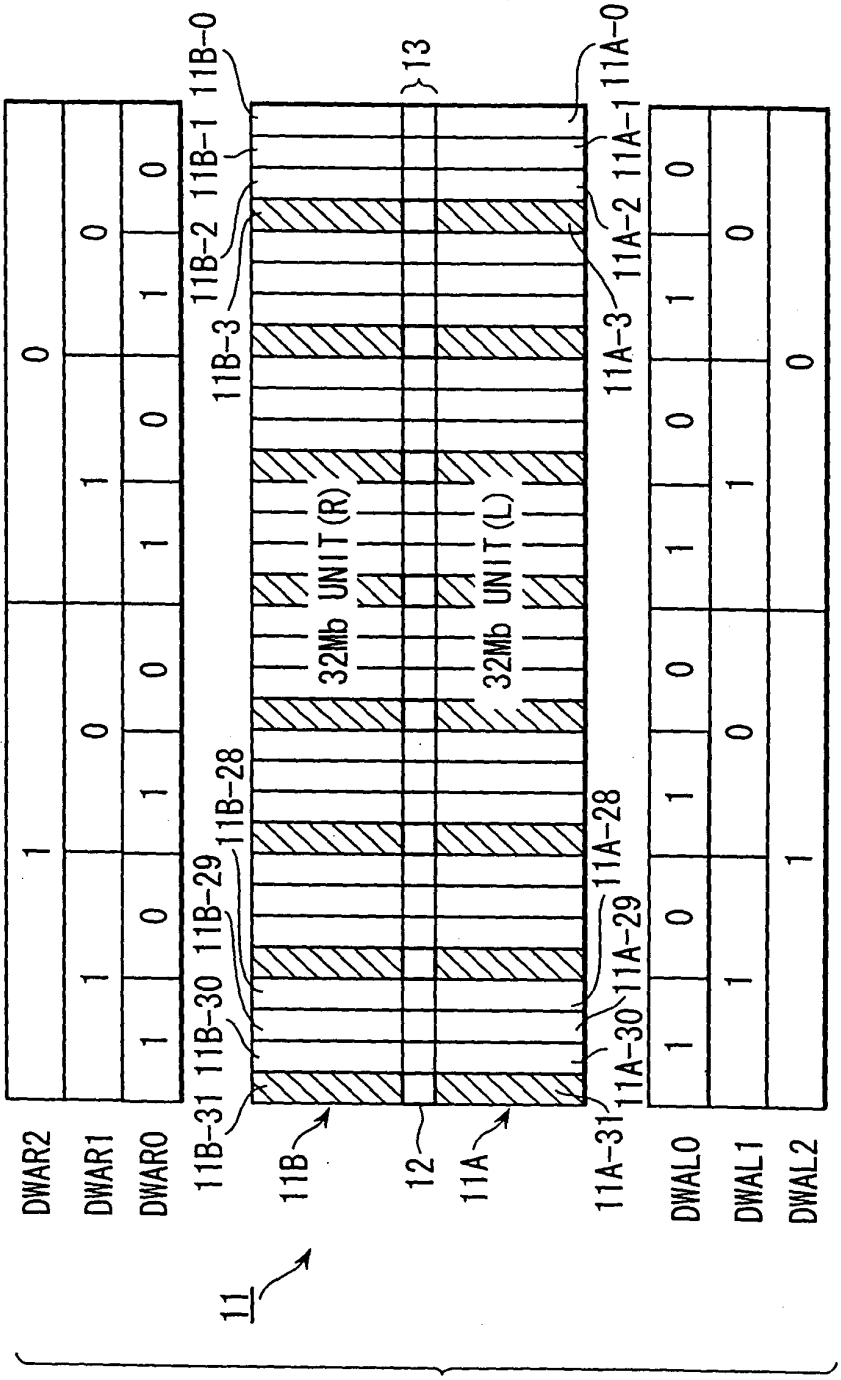

DWAR2
DWAR1
DWAR0
DWAL0
DWAL1
DWAL2
11
11B
12
11A
13
32Mb UNIT(R)
32Mb UNIT(L)
11B-0
11B-1
11B-2
11B-3
11B-28
11B-29
11B-30
11B-31
11A-0
11A-1
11A-2
11A-3
11A-28
11A-29
11A-30
11A-31

FIG. 2

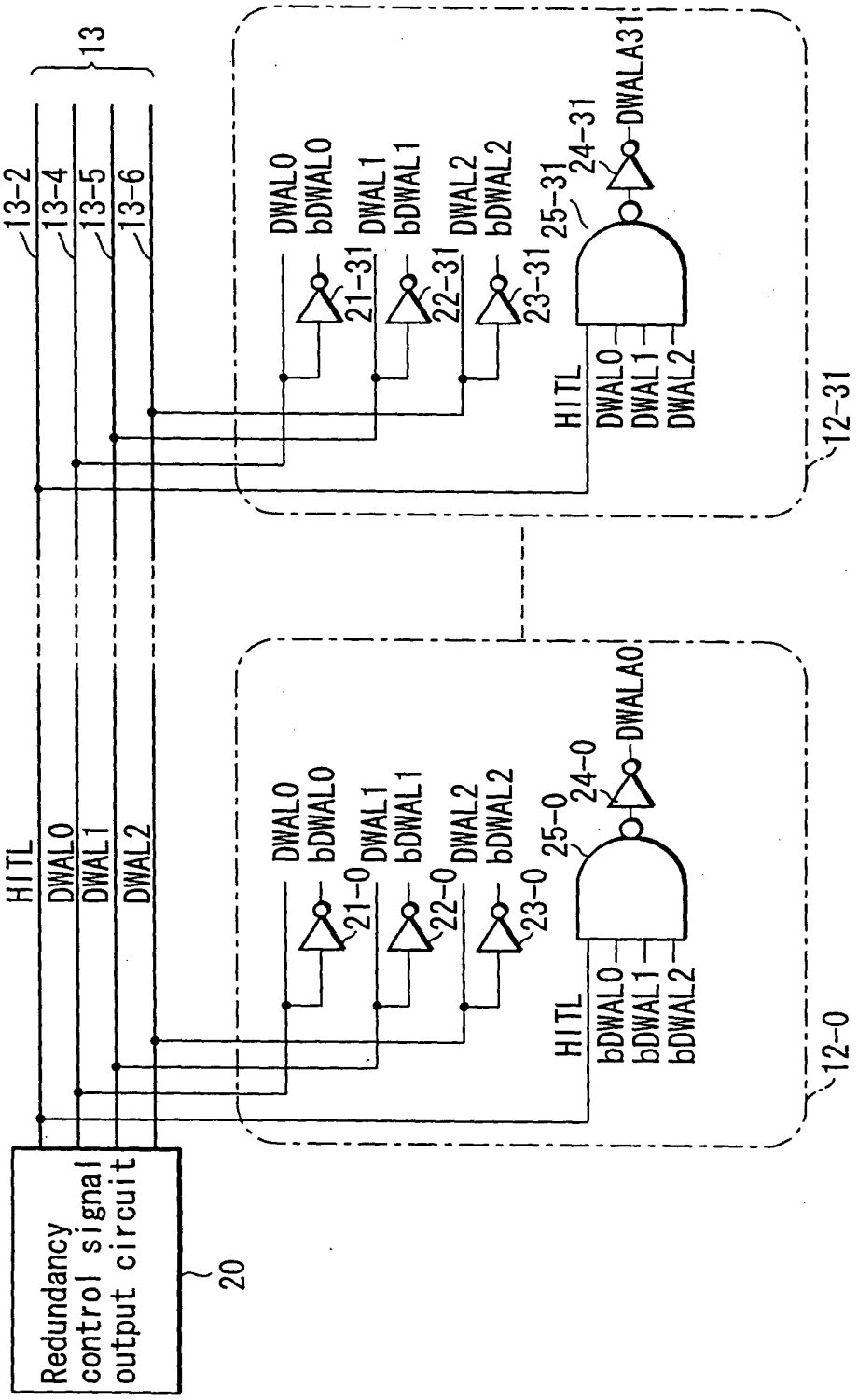

Redundancy control signal output circuit
20
HITL
DWAL0
DWAL1
DWAL2
13
13-2
13-4
13-5
13-6
DWAL0
bDWAL0
DWAL1
bDWAL1
DWAL2
bDWAL2
21-0
22-0
23-0
25-0
24-0
DWALA0
HITL
bDWAL0
bDWAL1
bDWAL2
12-0
21-31
22-31
23-31
25-31
24-31
DWALA31
HITL
DWAL0
DWAL1
DWAL2
12-31

FIG. 3

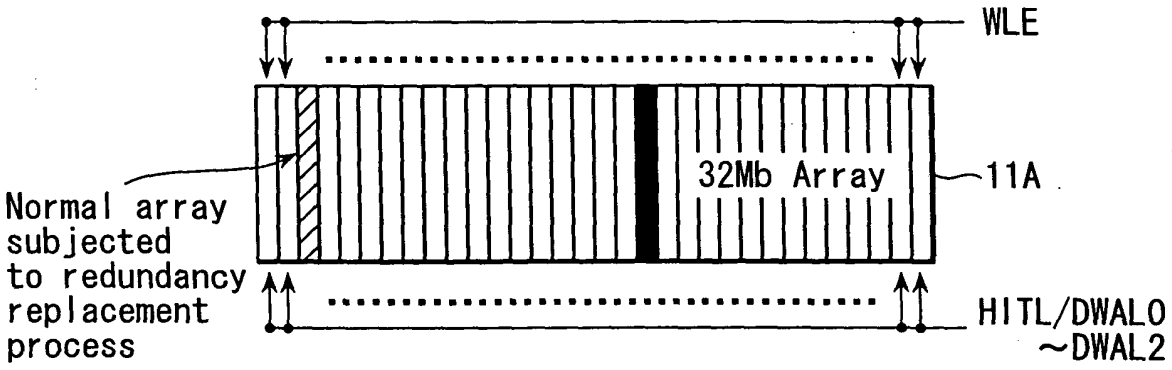

WLE
32Mb Array
11A
Normal array subjected to redundancy replacement process
HITL/DWAL0 ~DWAL2

FIG. 4A

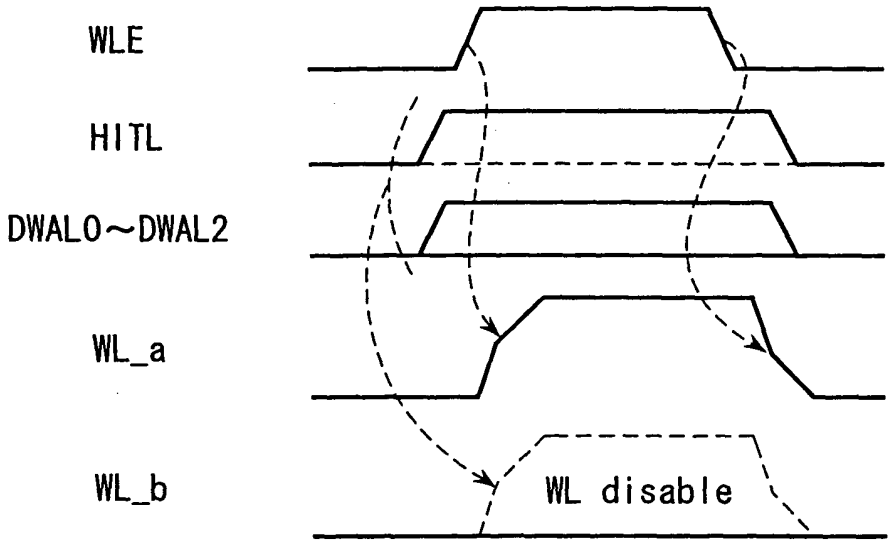

WLE
HITL
DWAL0~DWAL2
WL_a
WL_b
WL disable

FIG. 4B

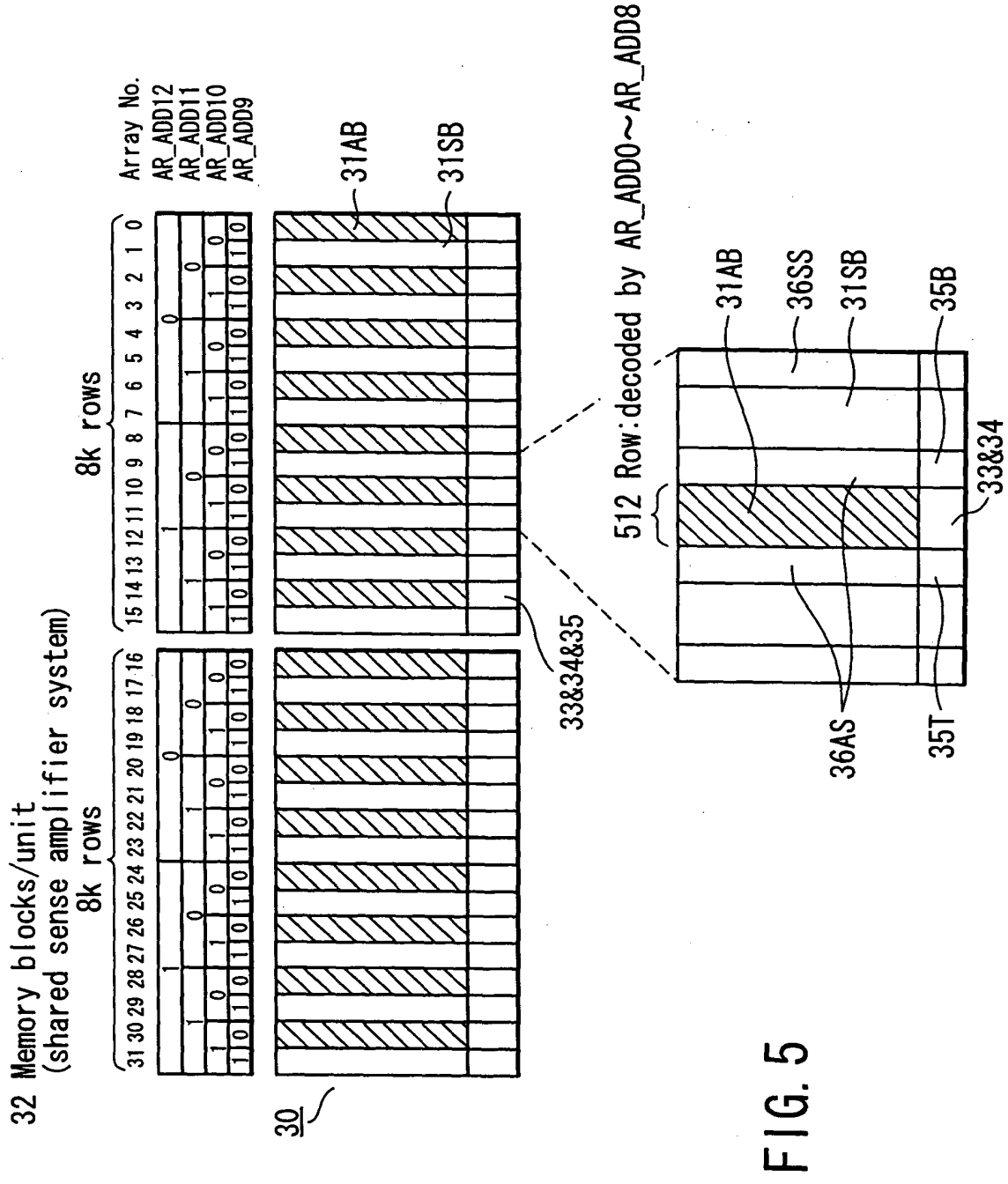
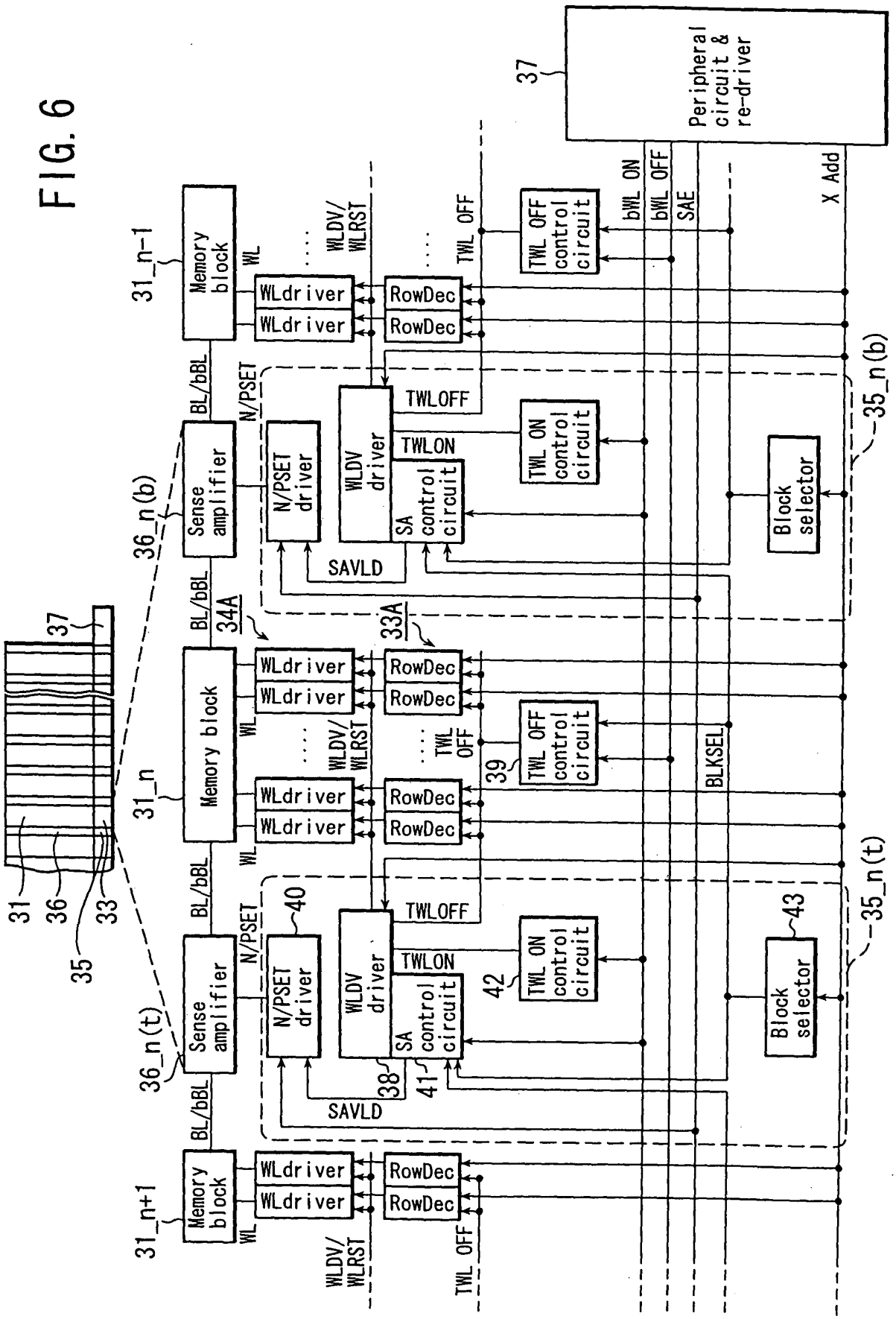

32 Memory blocks/unit
(shared sense amplifier system)
8k rows
8k rows
Array No.
AR_ADD12
AR_ADD11
AR_ADD10
AR_ADD9
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
30
31AB
31SB
33&34&35
512 Row:decoded by AR_ADD0~AR_ADD8
31AB
36SS
31SB
35B
33&34
36AS
35T

FIG. 5

FIG. 6


Peripheral circuit & re-driver
37
X Add
bWL ON
bWL OFF
SAE
BLKSEL
31_n-1
31_n
31_n+1
Memory block
WL
BL/bBL
WLdriver
RowDec
WLDV/WLRST
TWL OFF
TWL OFF control circuit
39
N/PSET
N/PSET driver
40
Sense amplifier
36_n(b)
36_n(t)
34A
33A
TWLOFF
TWLON
WLDV driver
SA control circuit
38
41
SAVLD
TWL ON control circuit
42
Block selector
43
35_n(b)
35_n(t)
31
36
33
35

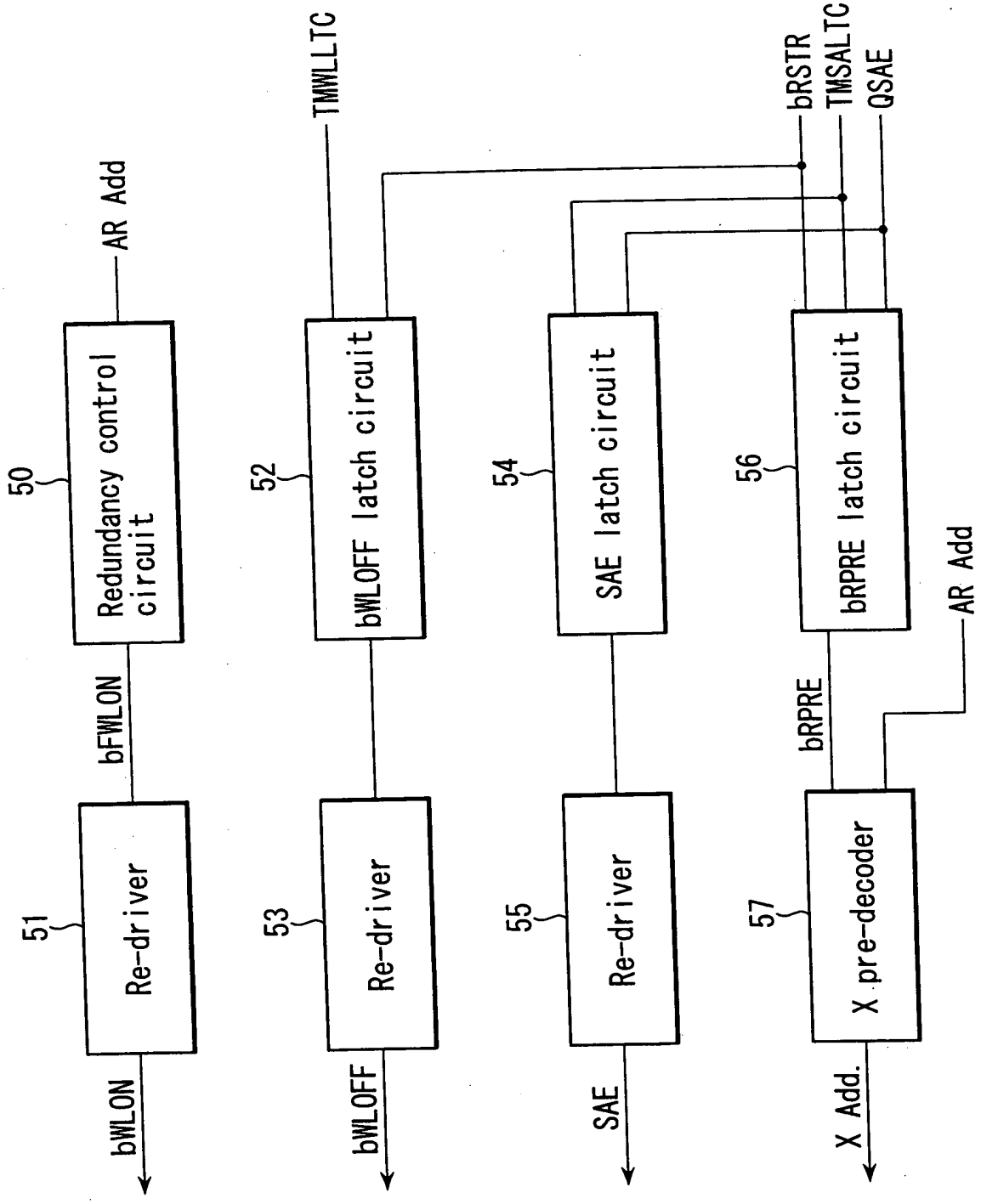

50
Redundancy control circuit
AR Add
bFWLON
51
Re-driver
bWLON
52
bWLOFF latch circuit
TMWLLTC
53
Re-driver
bWLOFF
54
SAE latch circuit
55
Re-driver
SAE
56
bRPRE latch circuit
bRSTR
TMSALTC
QSAE
bRPRE
57
X pre-decoder
AR Add
X Add.

FIG. 7

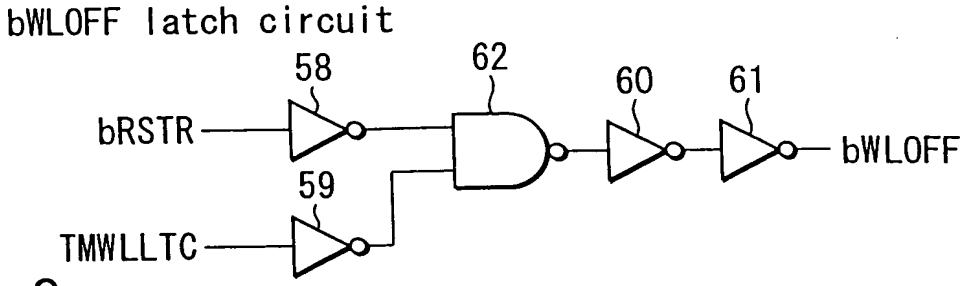


FIG. 8

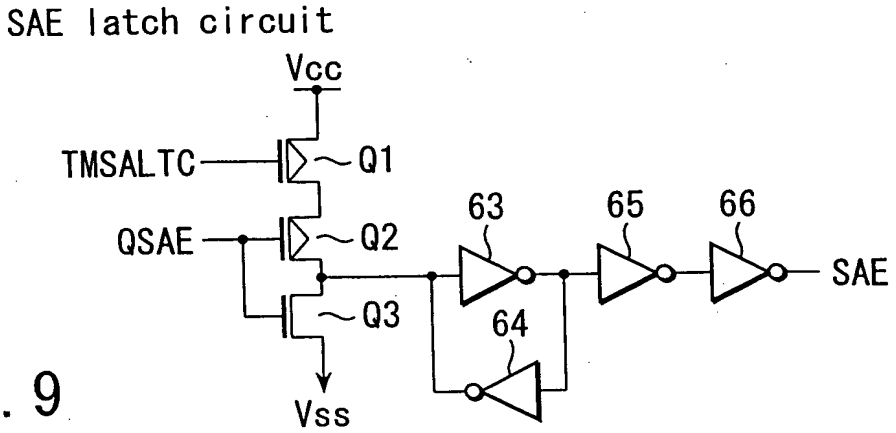


FIG. 9

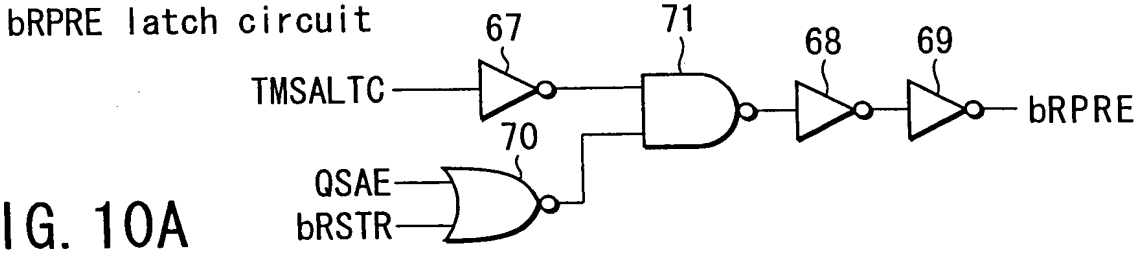


FIG. 10A

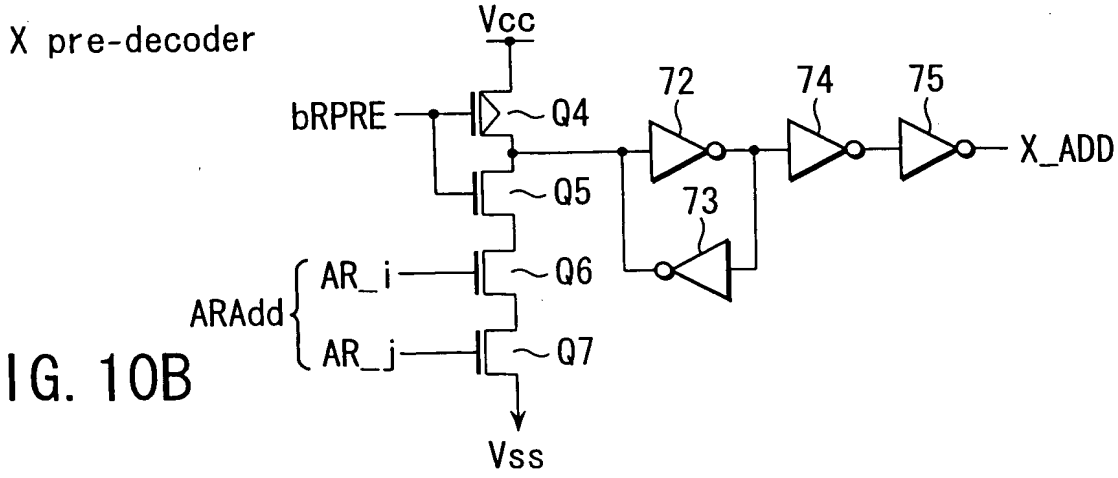


FIG. 10B

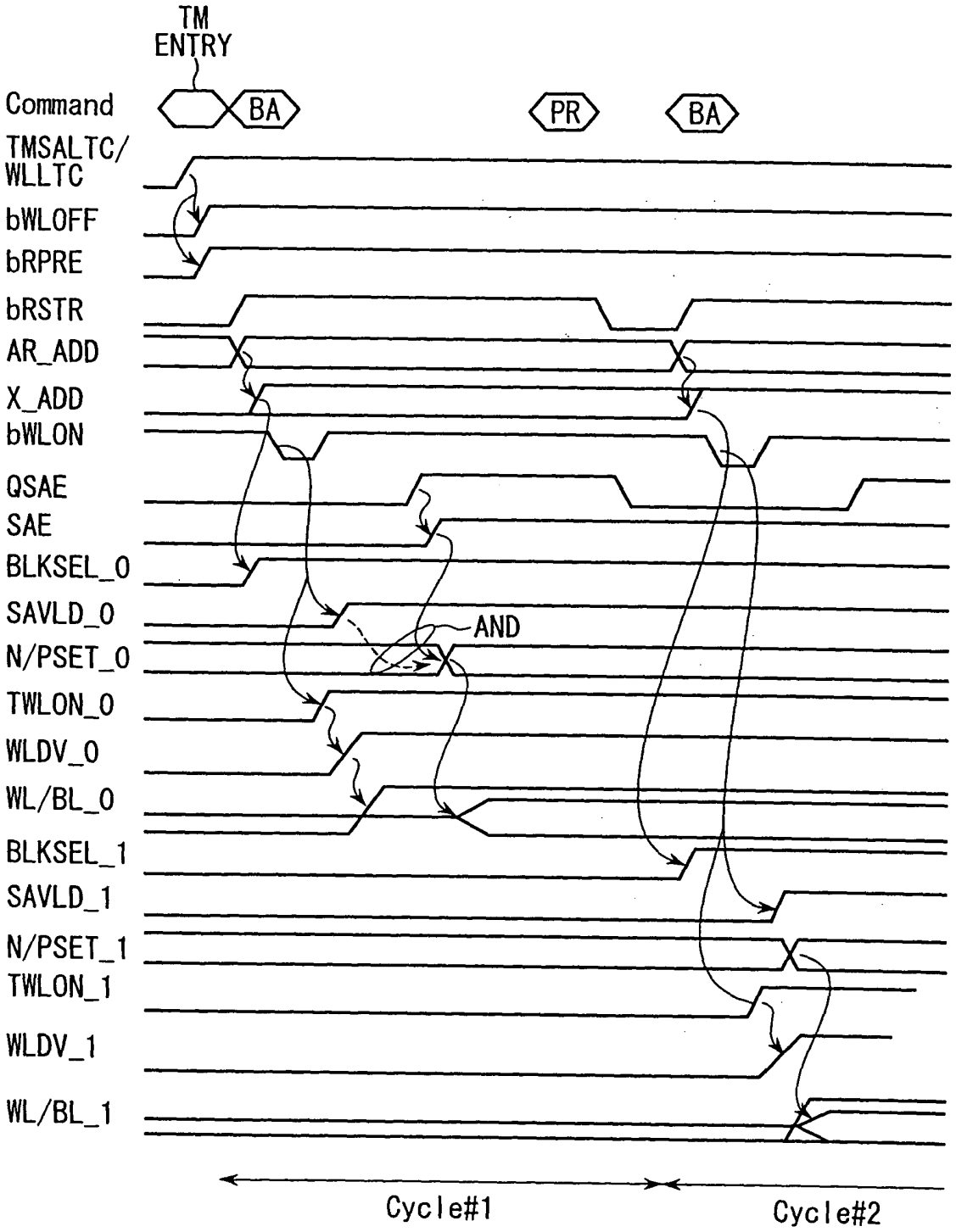

TM
ENTRY
Command
BA
PR
BA
TMSALTC/
WLLTC
bWLOFF
bRPRE
bRSTR
AR_ADD
X_ADD
bWLON
QSAE
SAE
BLKSEL_0
SAVLD_0
AND
N/PSET_0
TWLON_0
WLDV_0
WL/BL_0
BLKSEL_1
SAVLD_1
N/PSET_1
TWLON_1
WLDV_1
WL/BL_1
Cycle#1
Cycle#2

FIG. 11

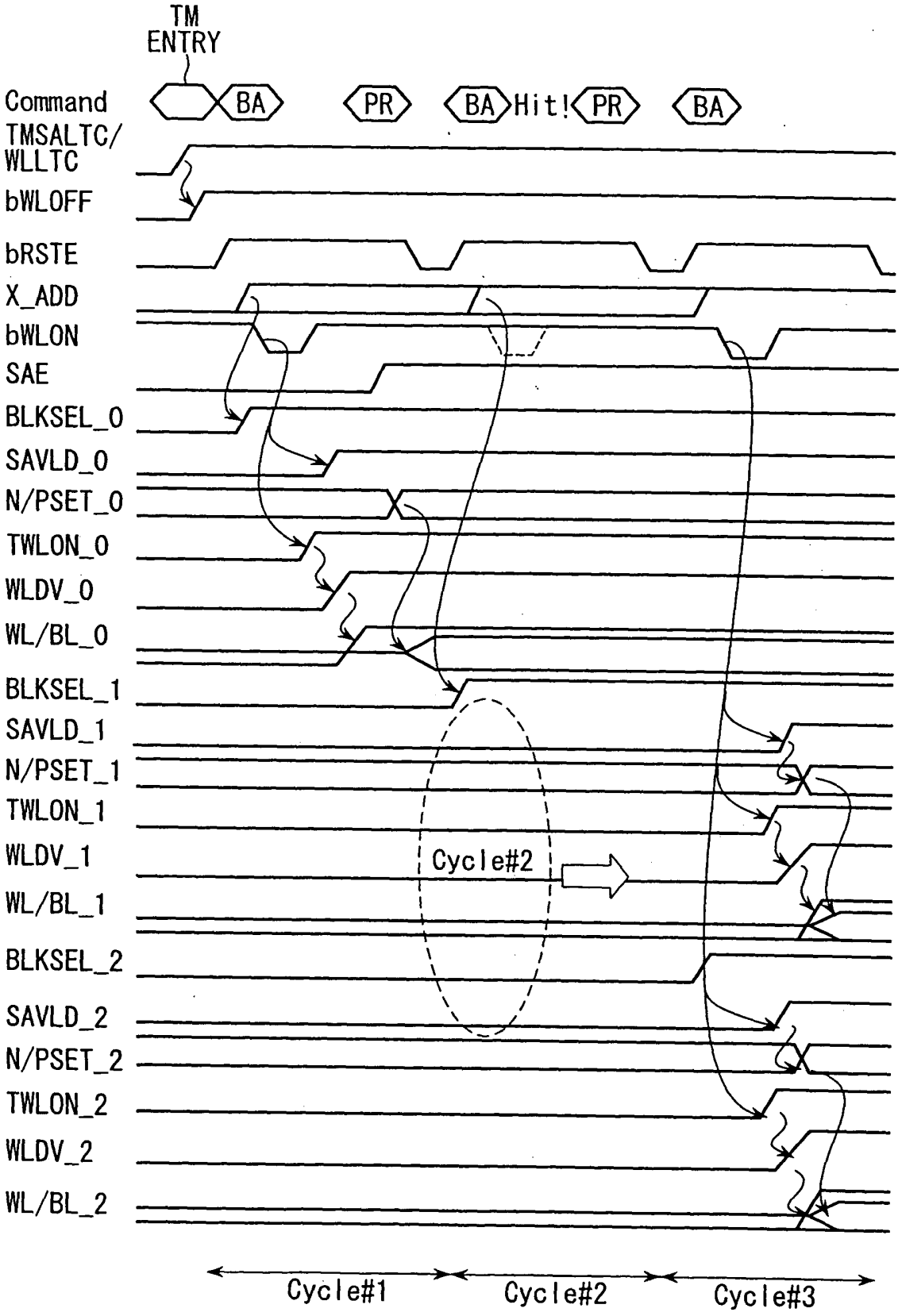

TM ENTRY
Command
BA
PR
BA
Hit!
PR
BA
TMSALTC/ WLLTC
bWLOFF
bRSTE
X_ADD
bWLON
SAE
BLKSEL_0
SAVLD_0
N/PSET_0
TWLON_0
WLDV_0
WL/BL_0
BLKSEL_1
SAVLD_1
N/PSET_1
TWLON_1
WLDV_1
WL/BL_1
BLKSEL_2
SAVLD_2
N/PSET_2
TWLON_2
WLDV_2
WL/BL_2
Cycle#2
Cycle#1
Cycle#2
Cycle#3

FIG. 12

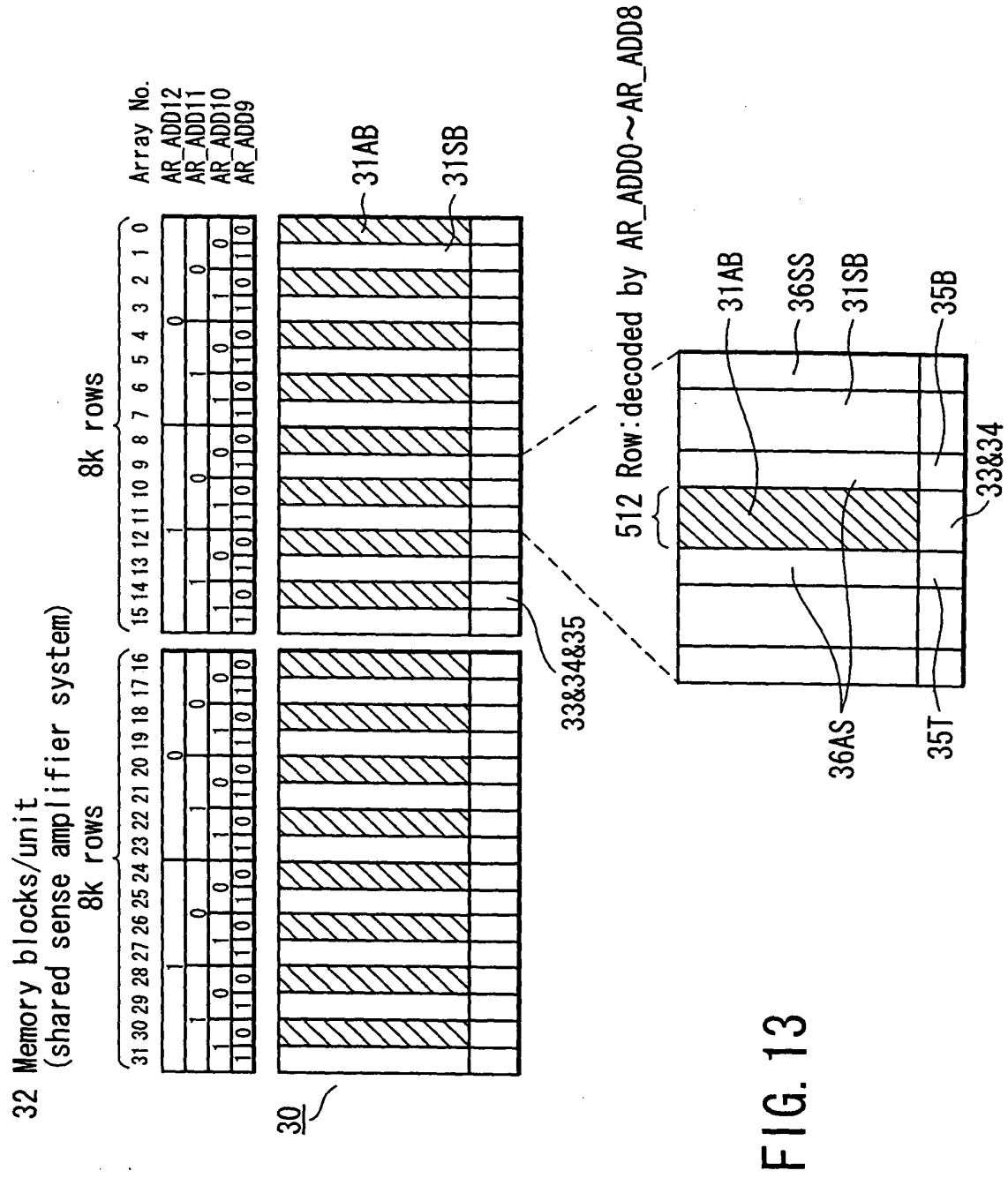
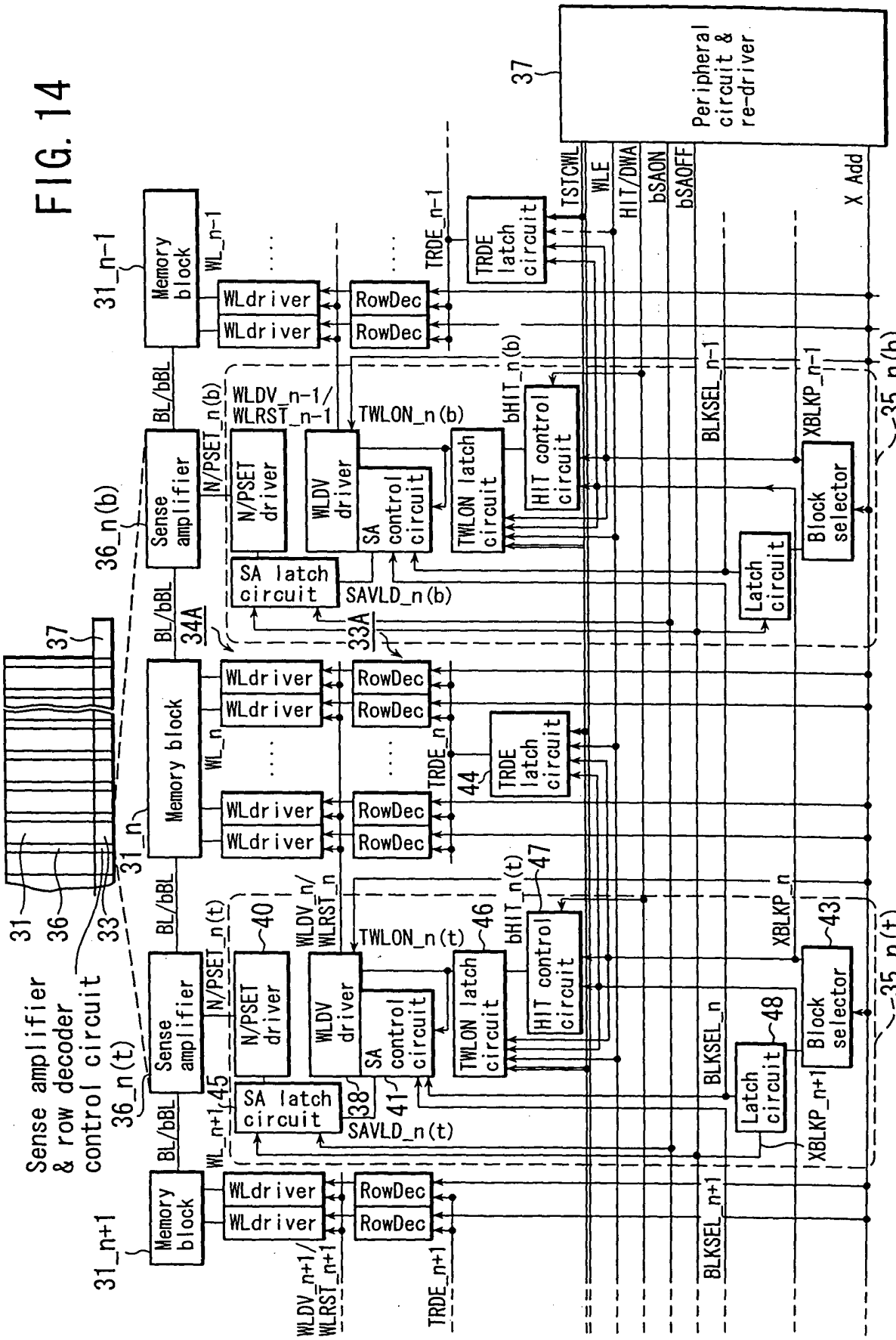

32 Memory blocks/unit
(shared sense amplifier system)
8k rows
8k rows
Array No.
AR_ADD12
AR_ADD11
AR_ADD10
AR_ADD9
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
30
31AB
31SB
33&34&35
512 Row:decoded by AR_ADD0~AR_ADD8
31AB
36SS
31SB
35B
33&34
36AS
35T

FIG. 13

FIG. 14


Peripheral circuit & re-driver
37
X Add
TSTCWL
WLE
HIT/DWA
bSAON
bSAOFF
Memory block
WLdriver
RowDec
TRDE latch circuit
HIT control circuit
TWLON latch circuit
WLDV driver
SA control circuit
N/PSET driver
Sense amplifier
SA latch circuit
Latch circuit
Block selector
BL/bBL
WL_n-1
WL_n
WL_n+1
TRDE_n-1
TRDE_n
TRDE_n+1
WLDV_n-1/WLRST_n-1
WLDV_n/WLRST_n
WLDV_n+1/WLRST_n+1
N/PSET_n(b)
N/PSET_n(t)
TWLON_n(b)
TWLON_n(t)
bHIT_n(b)
bHIT_n(t)
SAVLD_n(b)
SAVLD_n(t)
BLKSEL_n-1
BLKSEL_n
BLKSEL_n+1
XBLKP_n-1
XBLKP_n
XBLKP_n+1
31_n-1
31_n
31_n+1
31
33
33A
34A
35_n(b)
35_n(t)
36_n(b)
36_n(t)
38
40
41
43
44
45
46
47
48
Sense amplifier & row decoder control circuit

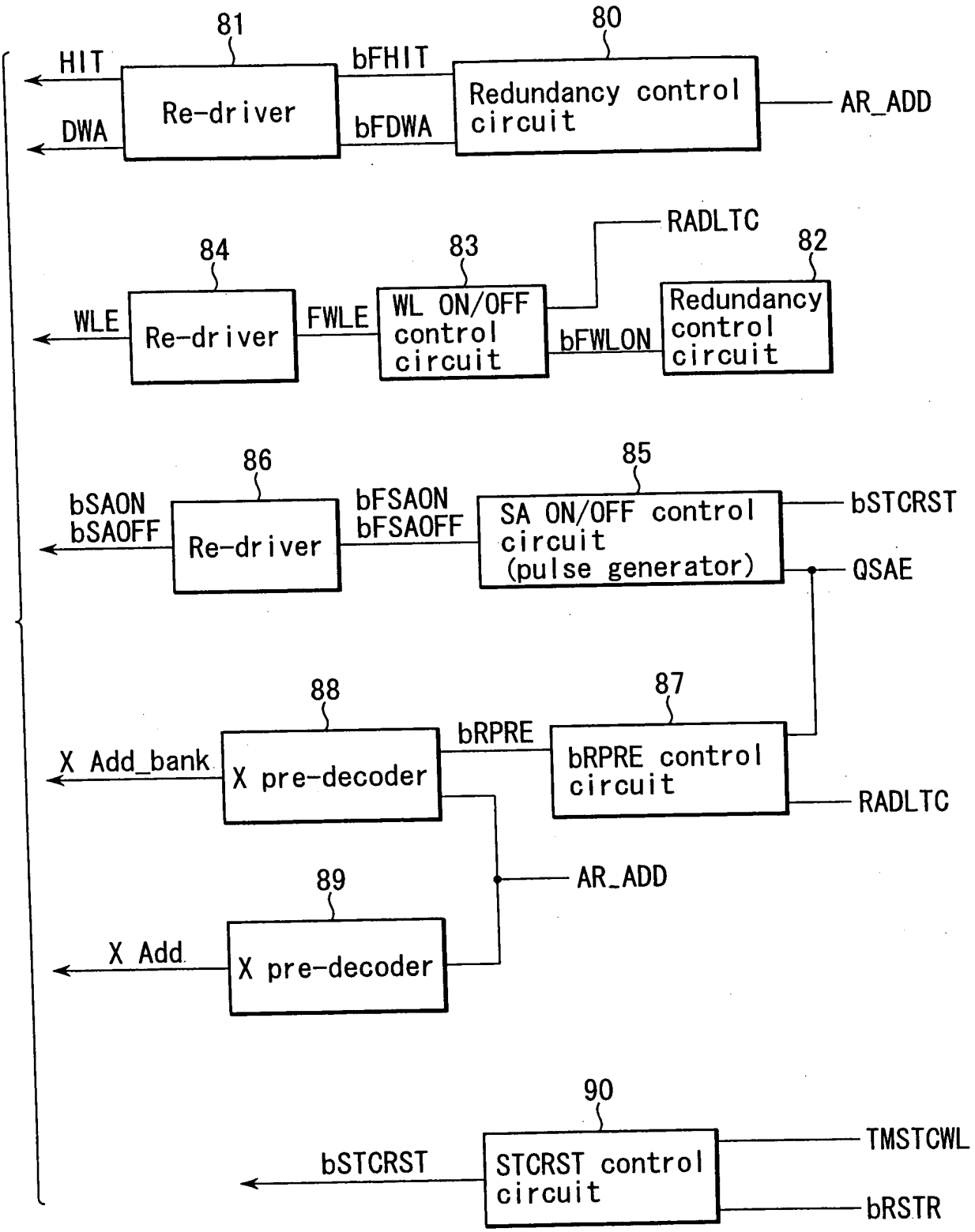

81
80
HIT
bFHIT
Re-driver
Redundancy control circuit
AR_ADD
DWA
bFDWA
RADLTC
84
83
82
WLE
FWLE
WL ON/OFF control circuit
Re-driver
Redundancy control circuit
bFWLON
86
85
bSAON
bSAOFF
bFSAON
bFSAOFF
Re-driver
SA ON/OFF control circuit (pulse generator)
bSTCRST
QSAE
88
87
X Add_bank
bRPRE
X pre-decoder
bRPRE control circuit
RADLTC
AR_ADD
89
X Add
X pre-decoder
90
bSTCRST
STCRST control circuit
TMSTCWL
bRSTR

FIG. 15

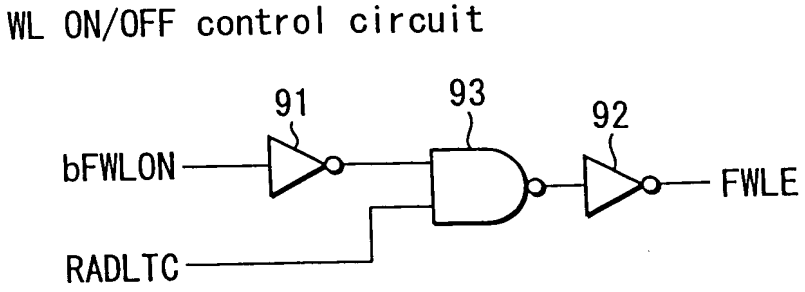


FIG. 16

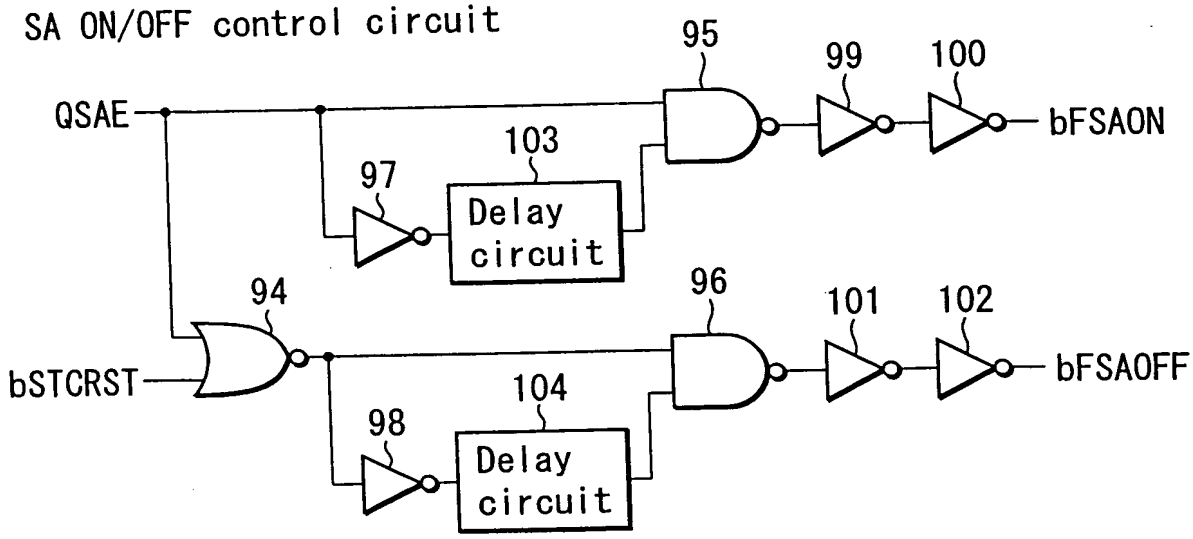


FIG. 17

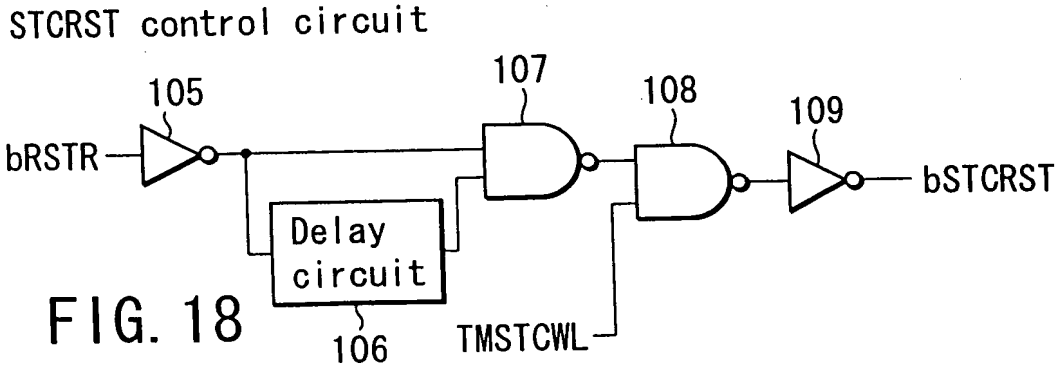


FIG. 18

BLKSEL latch circuit

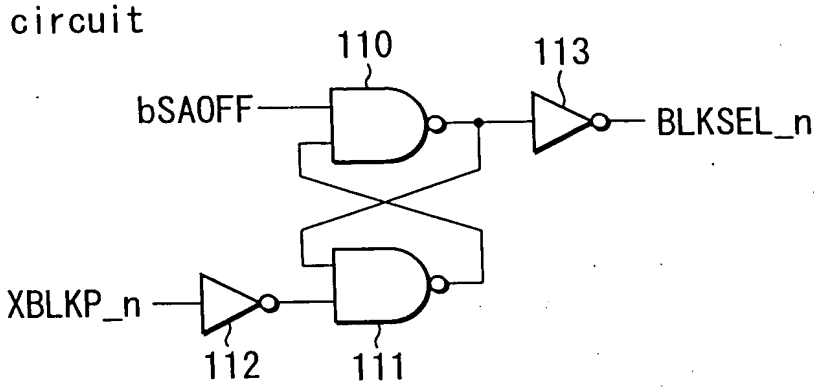


FIG. 19

TWLON latch circuit

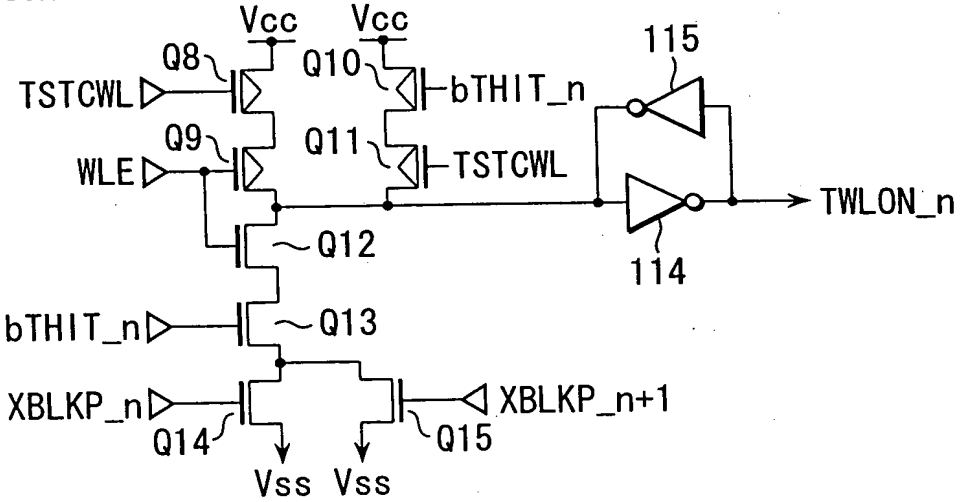


FIG. 20

SA control circuit

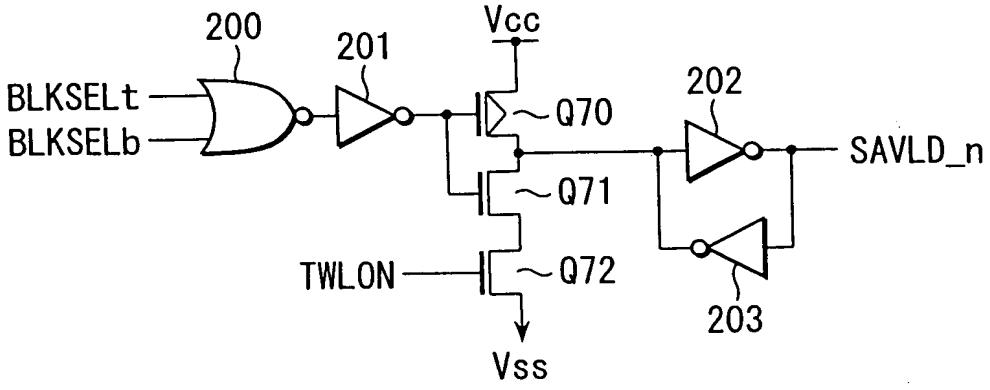


FIG. 21

SA latch circuit

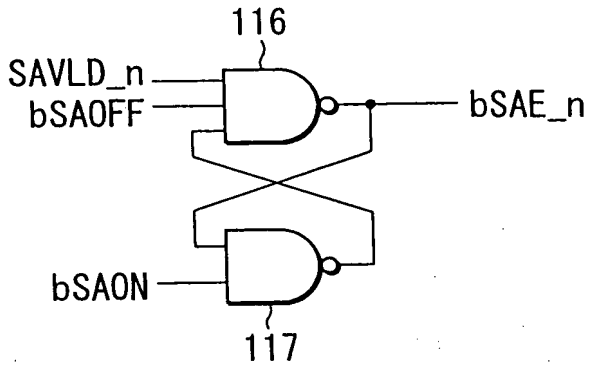


FIG. 22

TRDE latch circuit

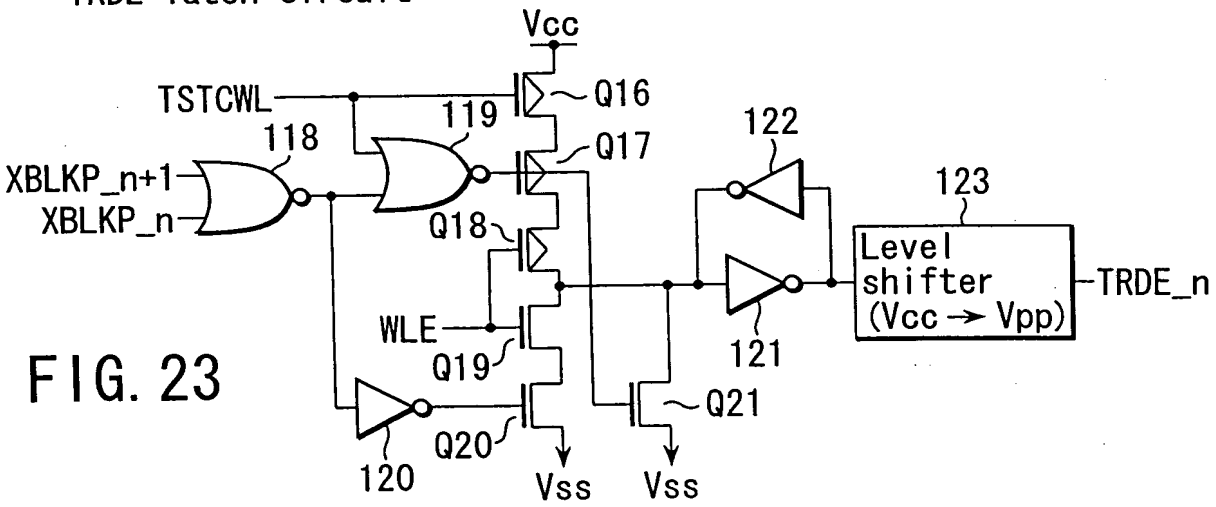


FIG. 23

HIT control circuit

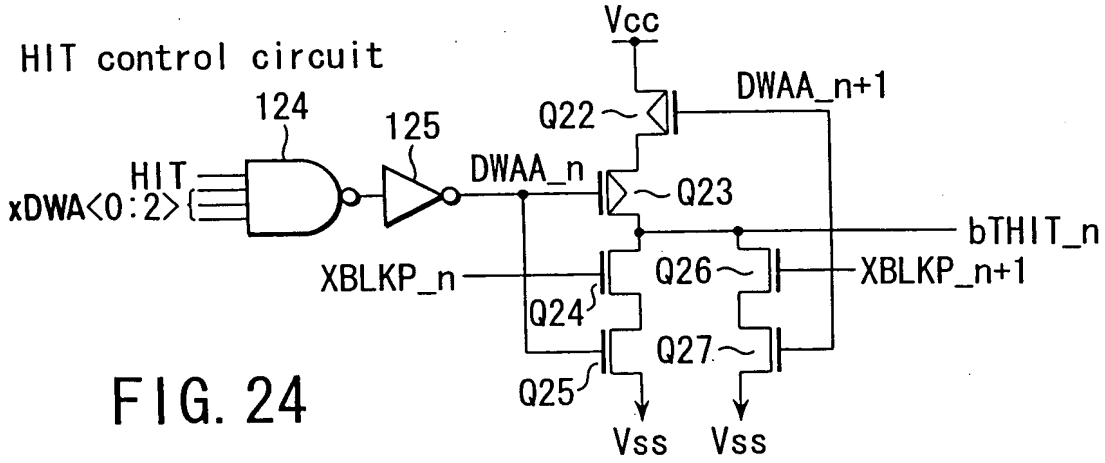


FIG. 24

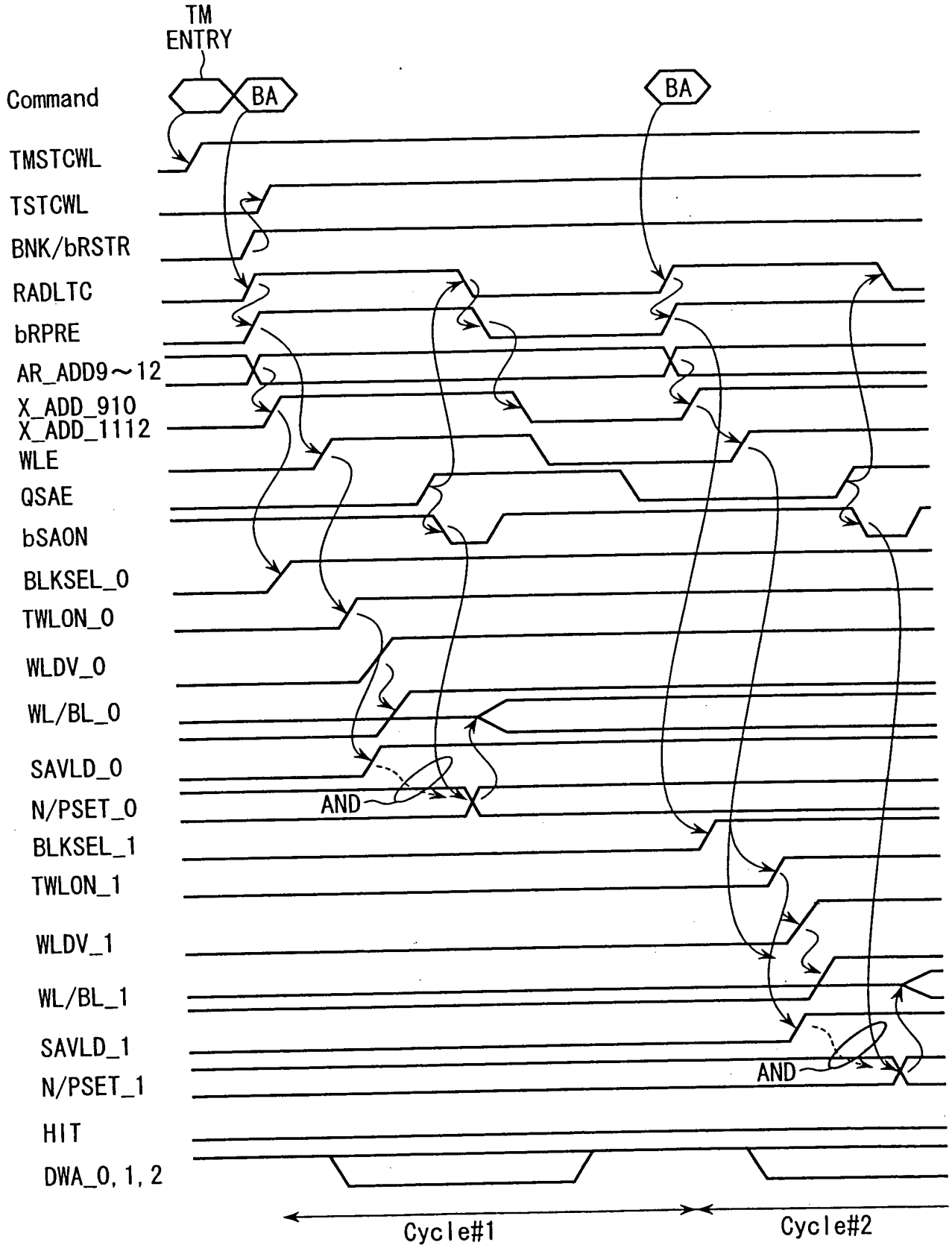

TM ENTRY
Command
BA
BA
TMSTCWL
TSTCWL
BNK/bRSTR
RADLTC
bRPRE
AR_ADD9～12
X_ADD_910
X_ADD_1112
WLE
QSAE
bSAON
BLKSEL_0
TWLON_0
WLDV_0
WL/BL_0
SAVLD_0
N/PSET_0
AND
BLKSEL_1
TWLON_1
WLDV_1
WL/BL_1
SAVLD_1
N/PSET_1
AND
HIT
DWA_0, 1, 2
Cycle#1
Cycle#2

FIG. 25

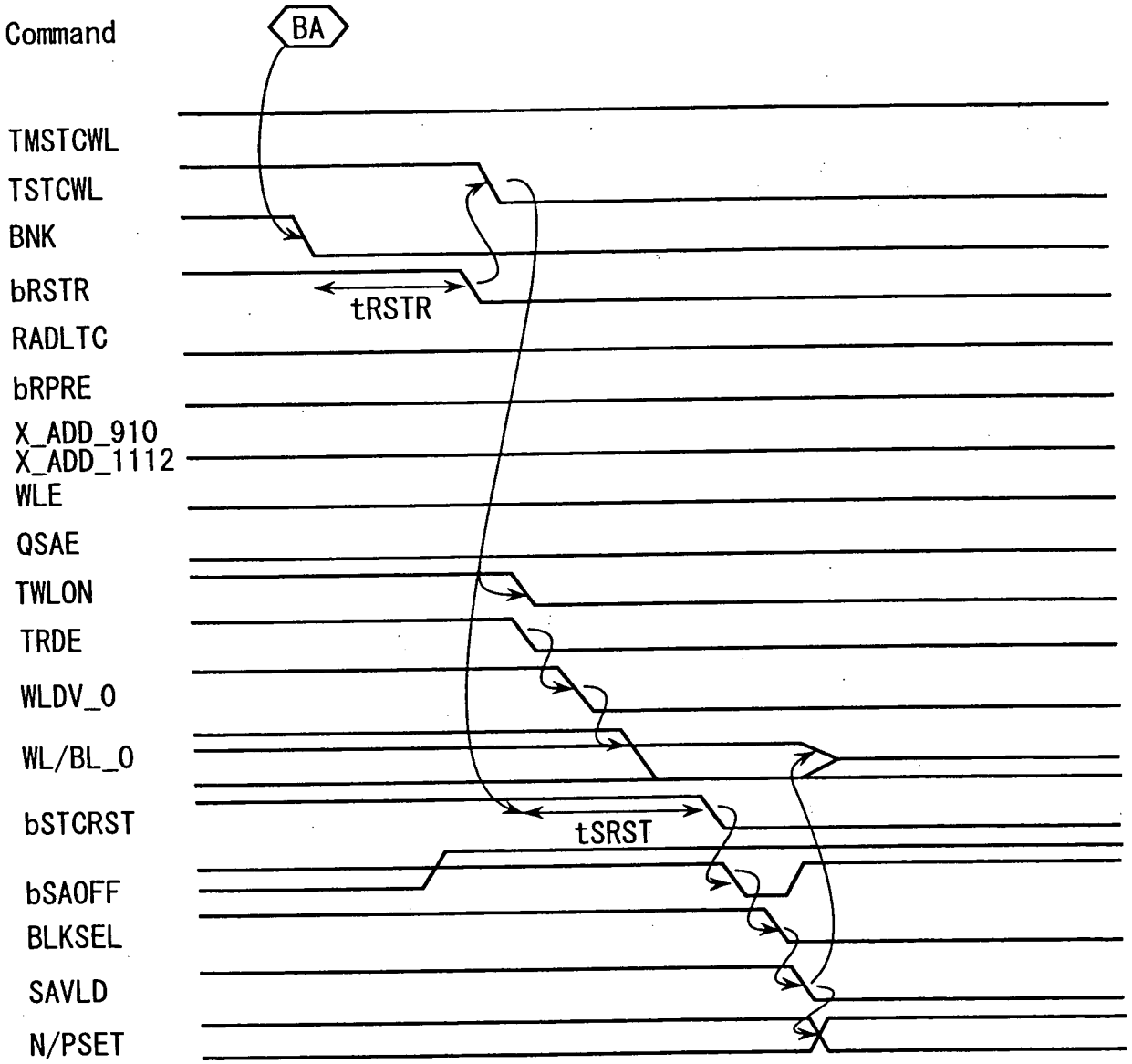

Command
BA
TMSTCWL
TSTCWL
BNK
bRSTR
tRSTR
RADLTC
bRPRE
X_ADD_910
X_ADD_1112
WLE
QSAE
TWLON
TRDE
WLDV_0
WL/BL_0
bSTCRST
tSRST
bSAOFF
BLKSEL
SAVLD
N/PSET

FIG. 26

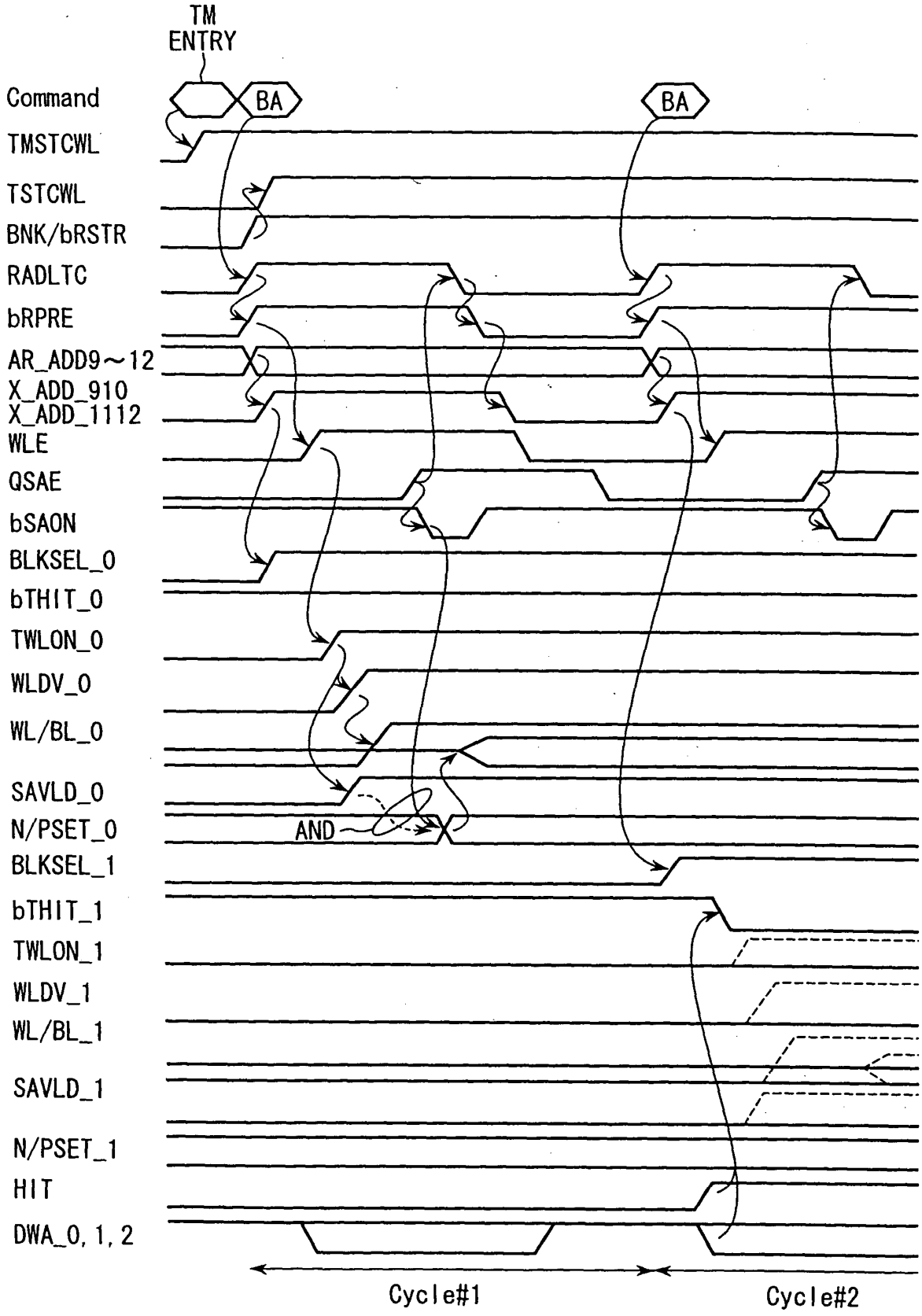

TM ENTRY
Command
BA
BA
TMSTCWL
TSTCWL
BNK/bRSTR
RADLTC
bRPRE
AR_ADD9~12
X_ADD_910
X_ADD_1112
WLE
QSAE
bSAON
BLKSEL_0
bTHIT_0
TWLON_0
WLDV_0
WL/BL_0
SAVLD_0
N/PSET_0
AND
BLKSEL_1
bTHIT_1
TWLON_1
WLDV_1
WL/BL_1
SAVLD_1
N/PSET_1
HIT
DWA_0, 1, 2
Cycle#1
Cycle#2

FIG. 27

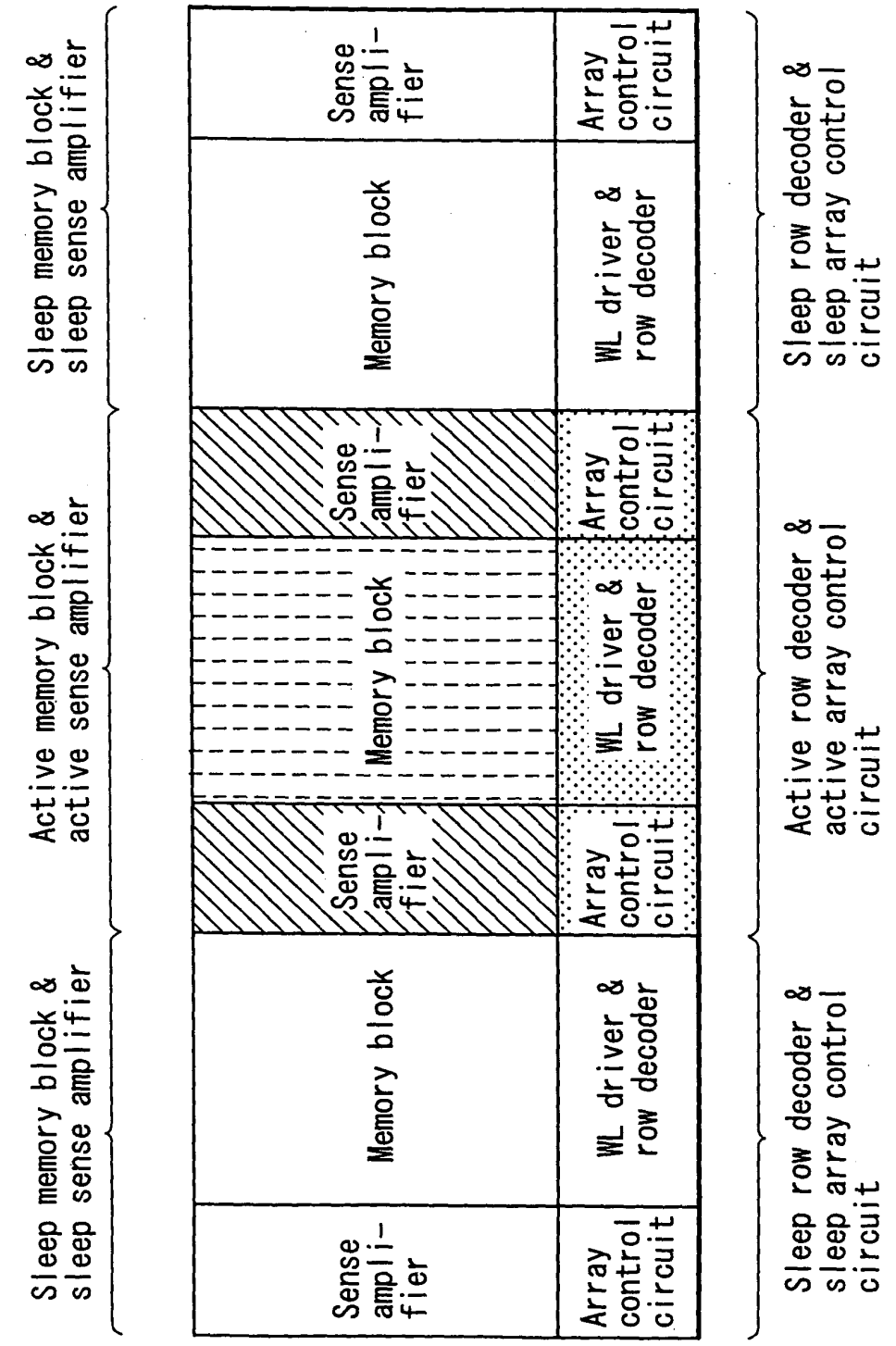

Sleep memory block & sleep sense amplifier
Active memory block & active sense amplifier
Sleep memory block & sleep sense amplifier
Sense amplifier
Memory block
Sense amplifier
Array control circuit
WL driver & row decoder
Array control circuit
WL driver & row decoder
Array control circuit
Sleep row decoder & sleep array control circuit
Active row decoder & active array control circuit
Sleep row decoder & sleep array control circuit

FIG. 28

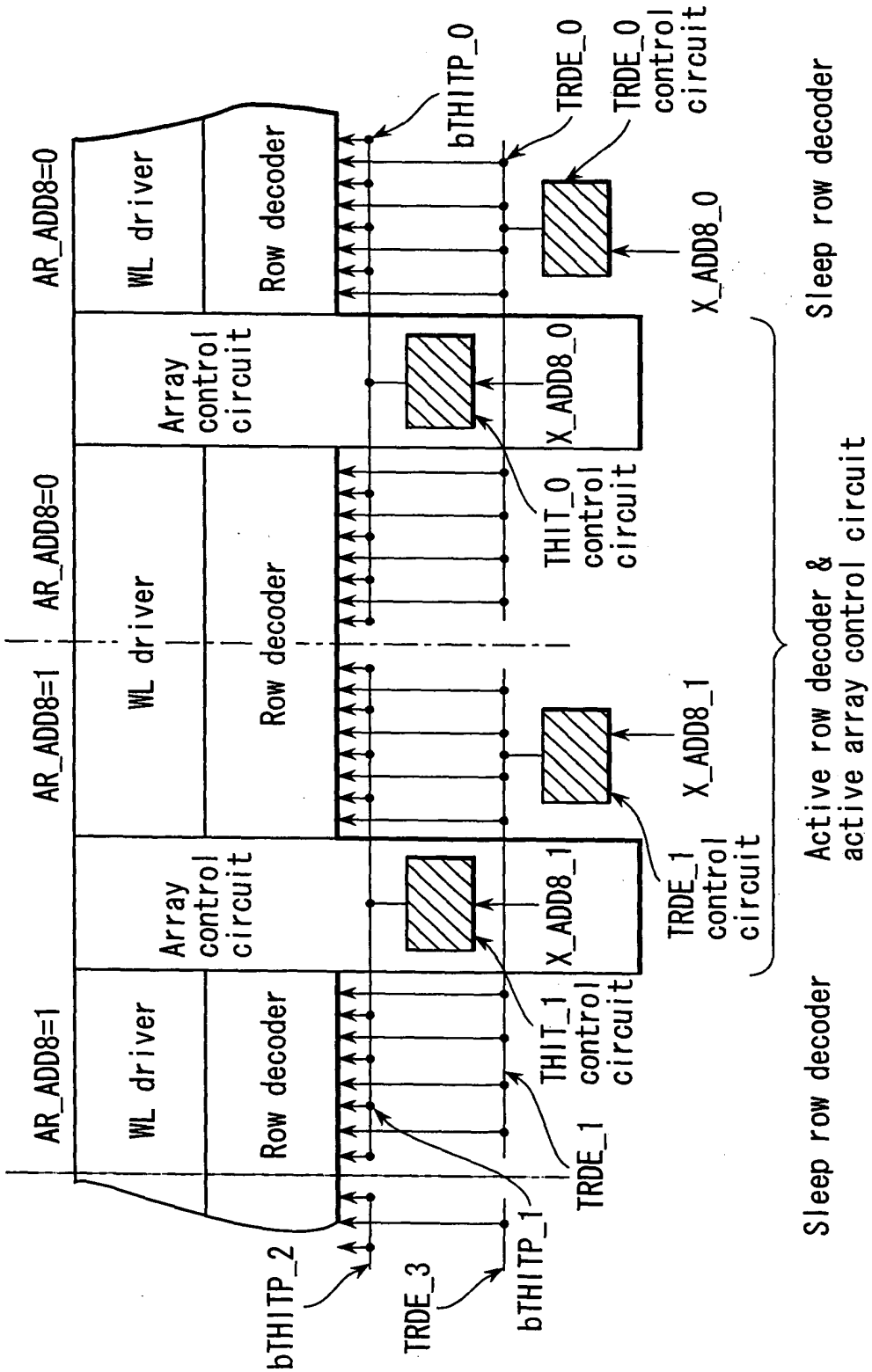
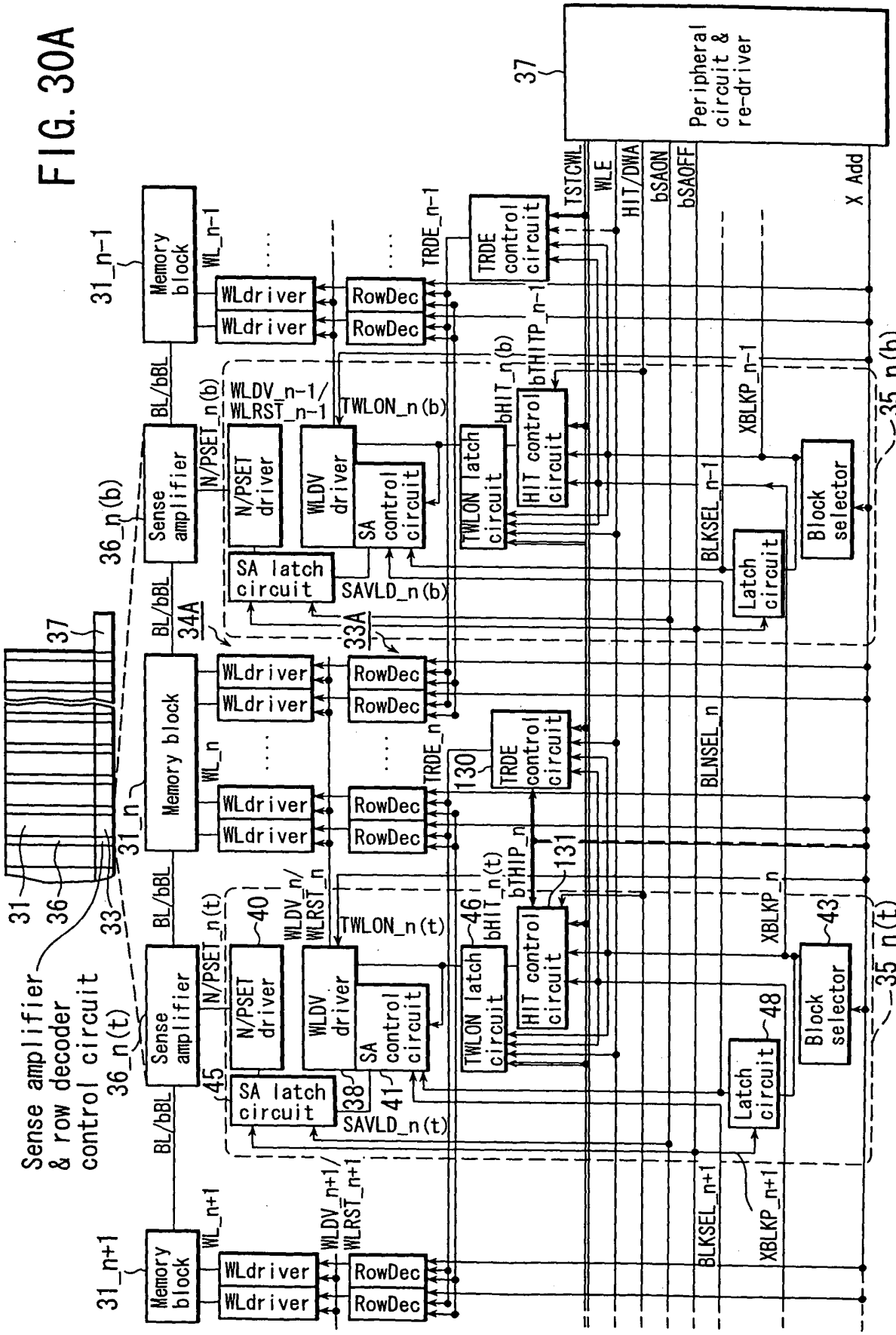

AR_ADD8=0
AR_ADD8=1
WL driver
Row decoder
Array control circuit
bTHITP_0
TRDE_0
TRDE_0 control circuit
X_ADD8_0
THIT_0 control circuit
X_ADD8_1
THIT_1 control circuit
TRDE_1 control circuit
bTHITP_2
TRDE_3
bTHITP_1
TRDE_1
Sleep row decoder
Active row decoder & active array control circuit

FIG. 29

FIG. 30A


Peripheral circuit & re-driver
37
X Add
TSTCWL
WLE
HIT/DWA
bSAON
bSAOFF
Memory block
31_n-1
31_n
31_n+1
WL_n-1
WL_n
WL_n+1
WLdriver
RowDec
TRDE_n-1
TRDE_n
TRDE control circuit
130
131
bTHITP_n-1
bTHIP_n
bTHIP_n(t)
HIT control circuit
bHIT_n(b)
bHIT_n(t)
46
TWLON latch circuit
WLDV_n-1/ WLRST_n-1
WLDV_n/ WLRST_n
WLDV_n+1/ WLRST_n+1
TWLON_n(b)
TWLON_n(t)
WLDV driver
SA control circuit
N/PSET_n(b)
N/PSET_n(t)
N/PSET driver
SA latch circuit
SAVLD_n(b)
SAVLD_n(t)
BL/bBL
Sense amplifier
36_n(b)
36_n(t)
34A
33A
33
31
36
37
40
41
45
38
BLKSEL_n-1
BLKSEL_n
BLKSEL_n+1
XBLKP_n-1
XBLKP_n
XBLKP_n+1
Latch circuit
48
Block selector
43
35_n(b)
35_n(t)
Sense amplifier & row decoder control circuit

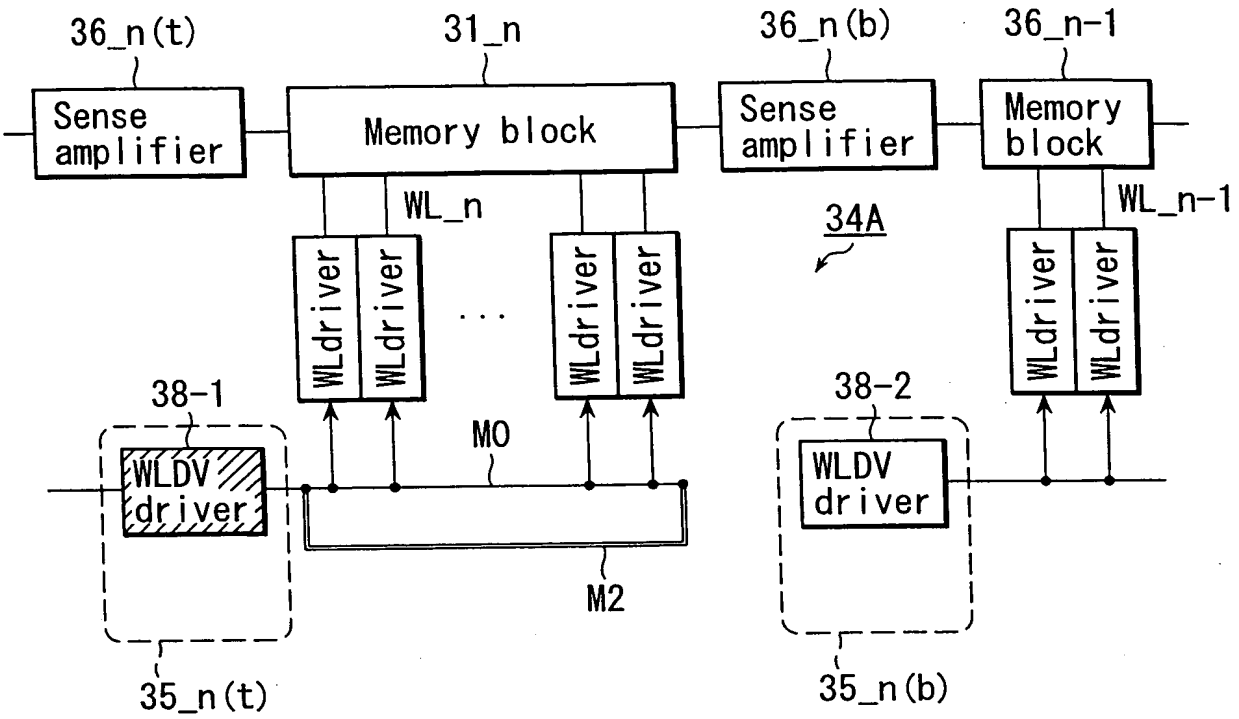


FIG. 30B

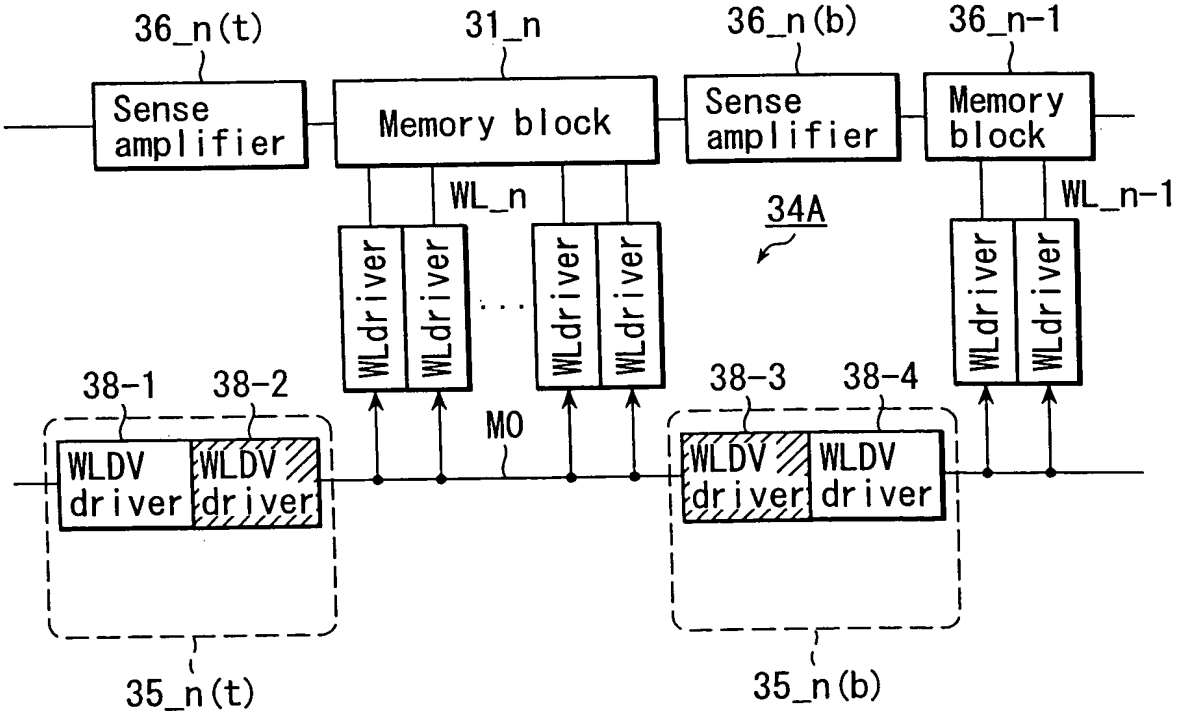


FIG. 30C

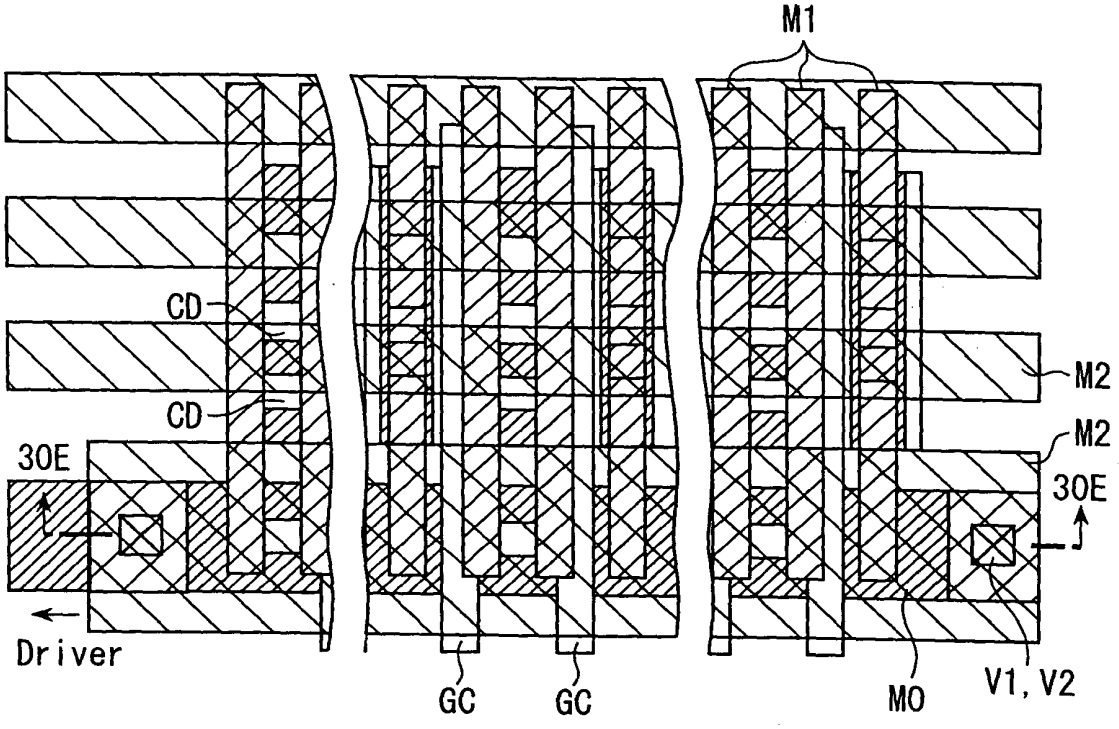


FIG. 30D

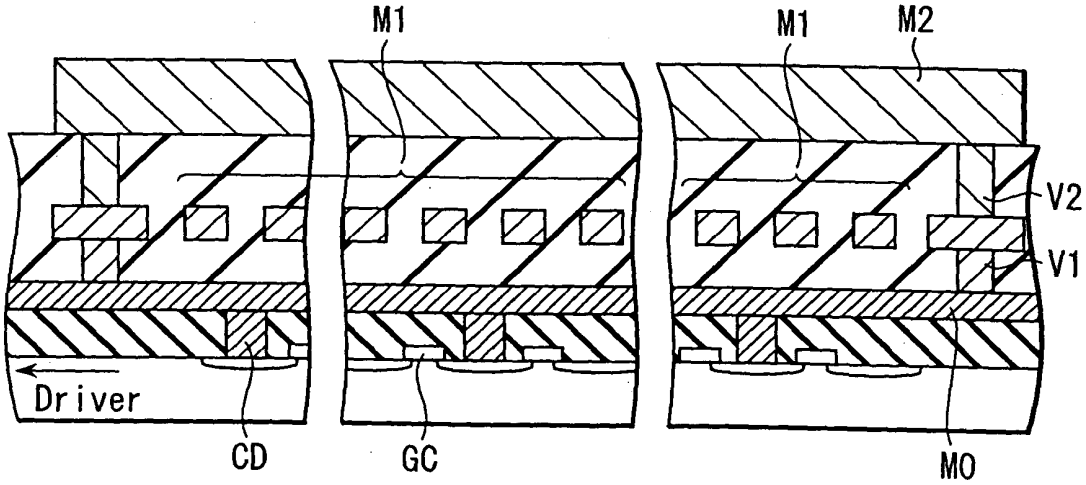


FIG. 30E

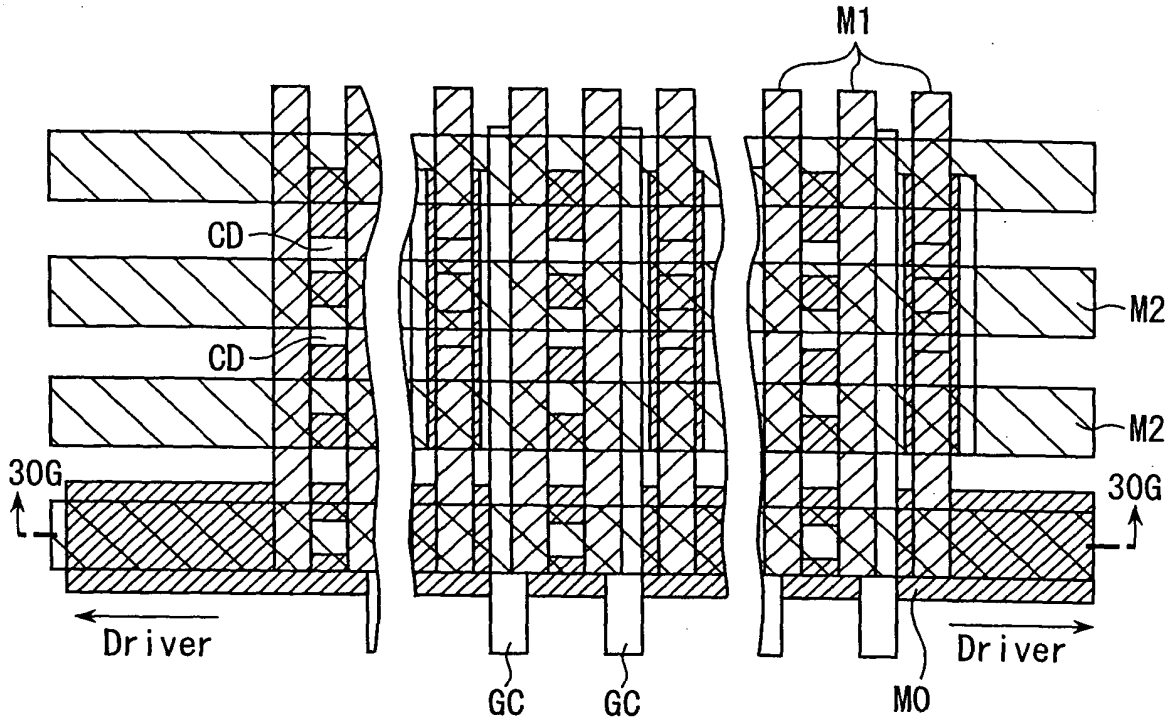


FIG. 30F

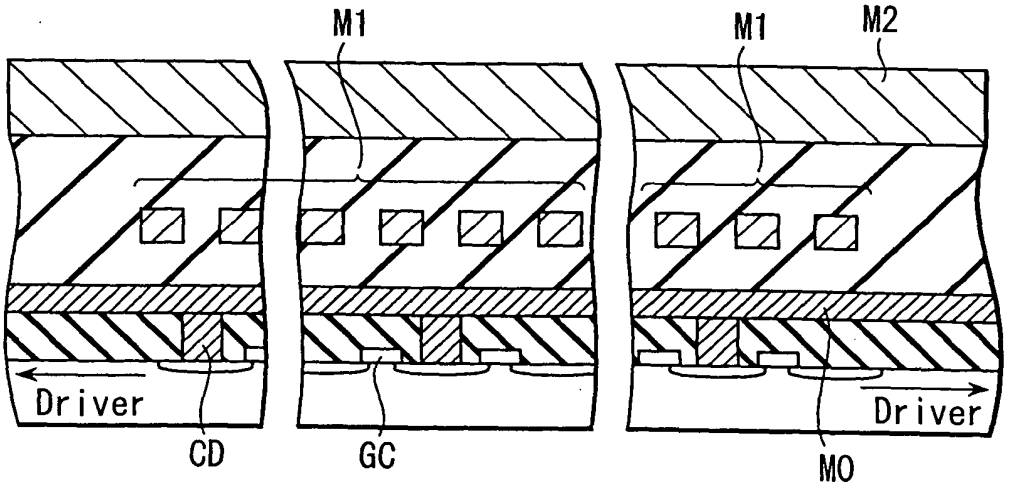


FIG. 30G

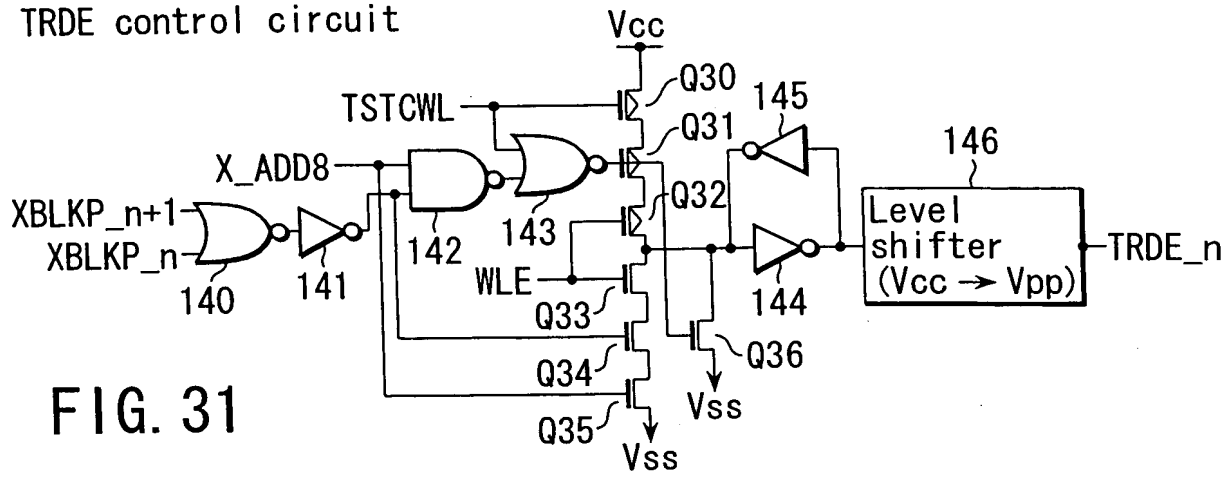


FIG. 31

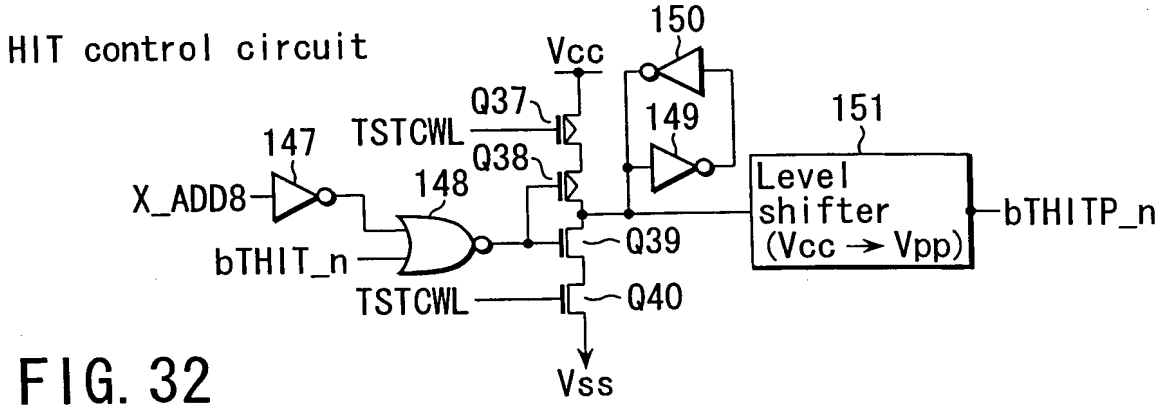


FIG. 32

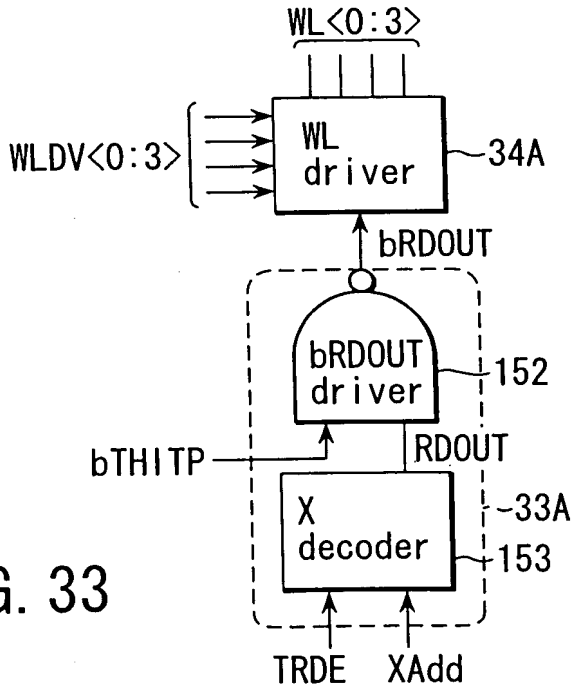


FIG. 33

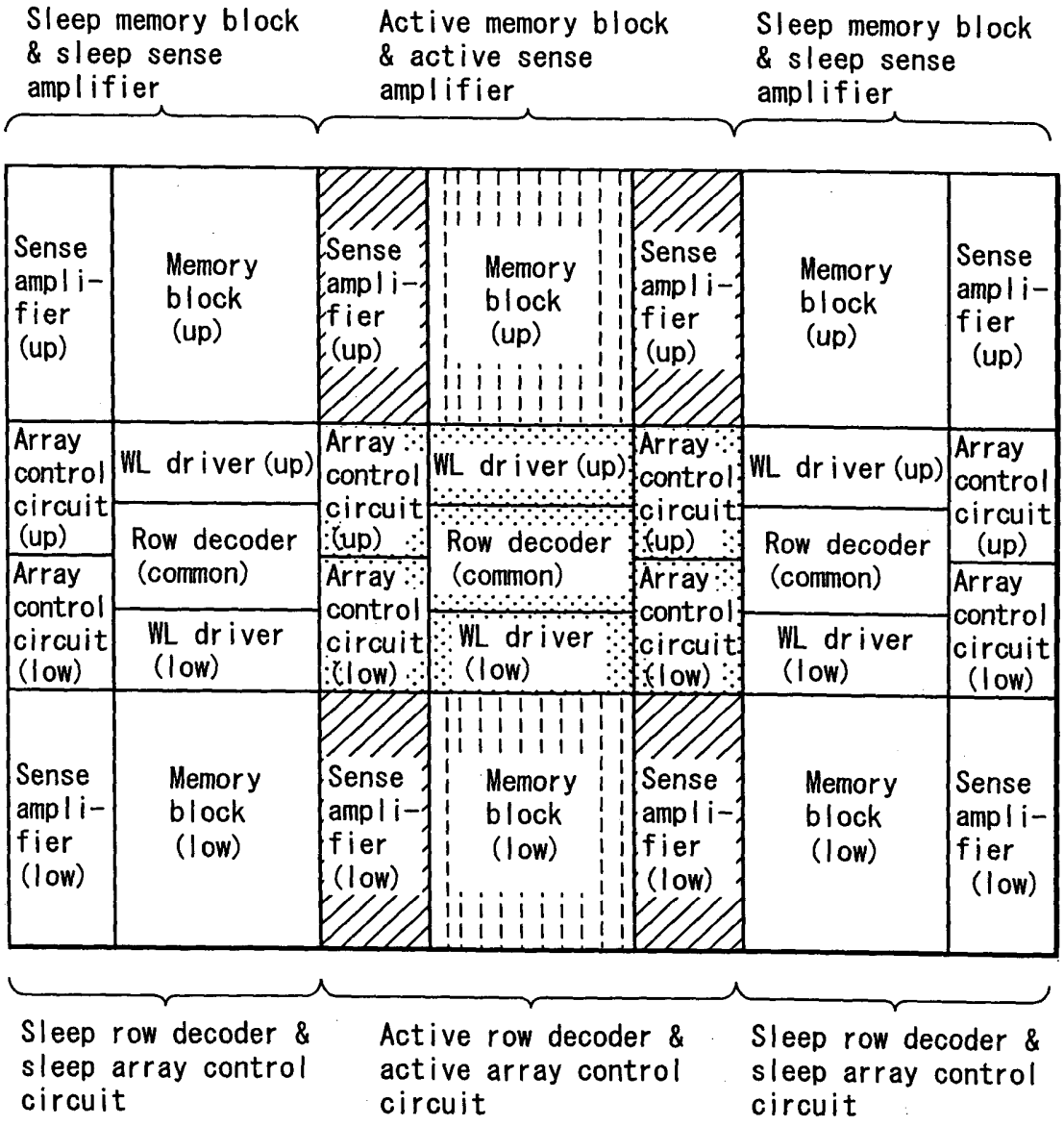

Sleep memory block & sleep sense amplifier
Active memory block & active sense amplifier
Sleep memory block & sleep sense amplifier
Sense amplifier (up)
Memory block (up)
Sense amplifier (up)
Memory block (up)
Sense amplifier (up)
Memory block (up)
Sense amplifier (up)
Array control circuit (up)
WL driver (up)
Array control circuit (up)
WL driver (up)
Array control circuit (up)
WL driver (up)
Array control circuit (up)
Row decoder (common)
Row decoder (common)
Row decoder (common)
Array control circuit (low)
WL driver (low)
Array control circuit (low)
WL driver (low)
Array control circuit (low)
WL driver (low)
Array control circuit (low)
Sense amplifier (low)
Memory block (low)
Sense amplifier (low)
Memory block (low)
Sense amplifier (low)
Memory block (low)
Sense amplifier (low)
Sleep row decoder & sleep array control circuit
Active row decoder & active array control circuit
Sleep row decoder & sleep array control circuit

FIG. 34

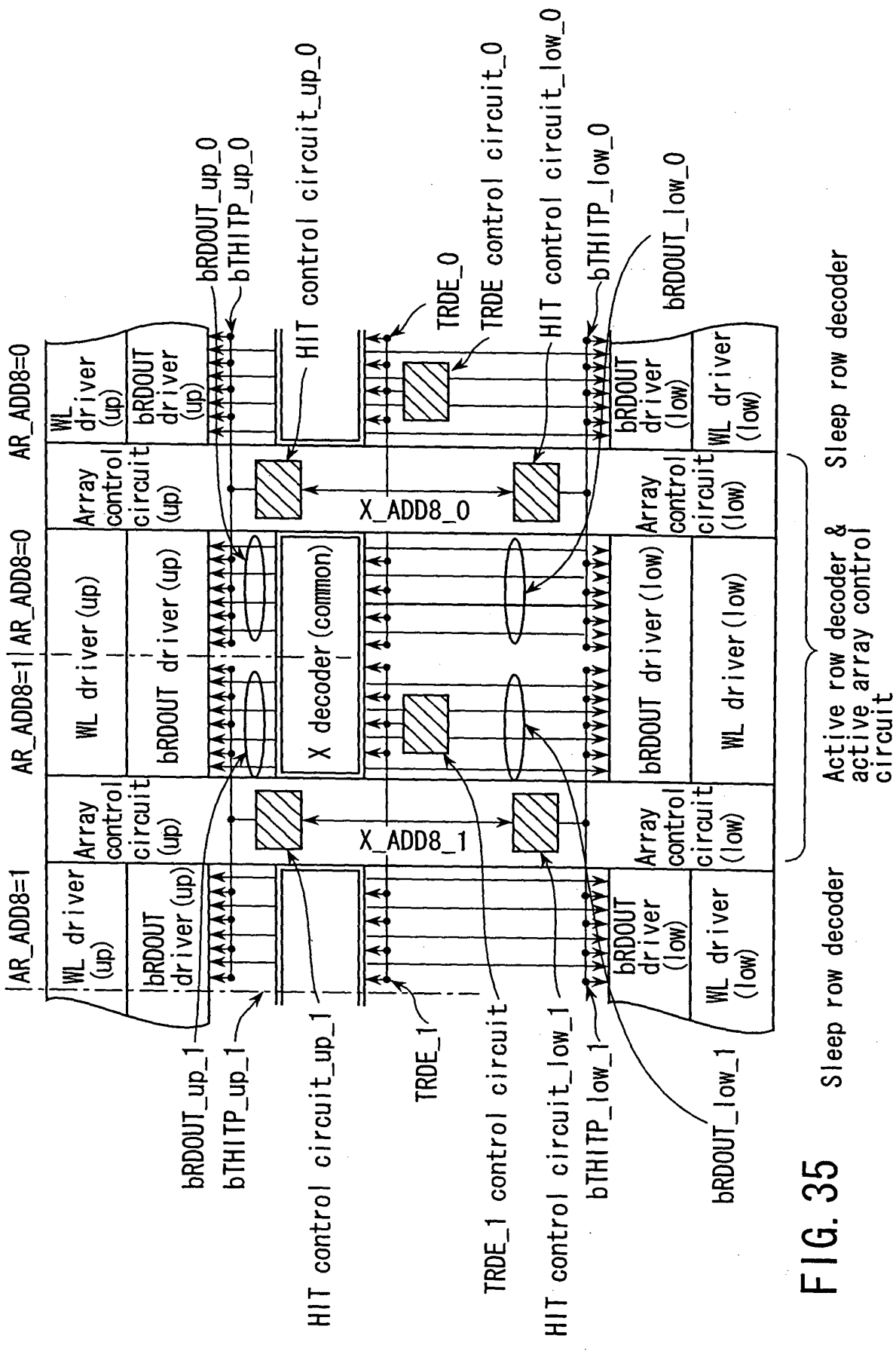

AR_ADD8=1
AR_ADD8=1
AR_ADD8=0
AR_ADD8=0
AR_ADD8=0
WL driver (up)
bRDOUT driver (up)
Array control circuit (up)
WL driver (up)
bRDOUT driver (up)
Array control circuit (up)
X decoder (common)
WL driver (low)
bRDOUT driver (low)
Array control circuit (low)
WL driver (low)
bRDOUT driver (low)
Array control circuit (low)
X_ADD8_0
X_ADD8_1
bRDOUT_up_0
bTHITP_up_0
HIT control circuit_up_0
TRDE_0
TRDE control circuit_0
HIT control circuit_low_0
bTHITP_low_0
bRDOUT_low_0
bRDOUT_up_1
bTHITP_up_1
HIT control circuit_up_1
TRDE_1
TRDE_1 control circuit
HIT control circuit_low_1
bTHITP_low_1
bRDOUT_low_1
Sleep row decoder
Active row decoder & active array control circuit
Sleep row decoder

FIG. 35

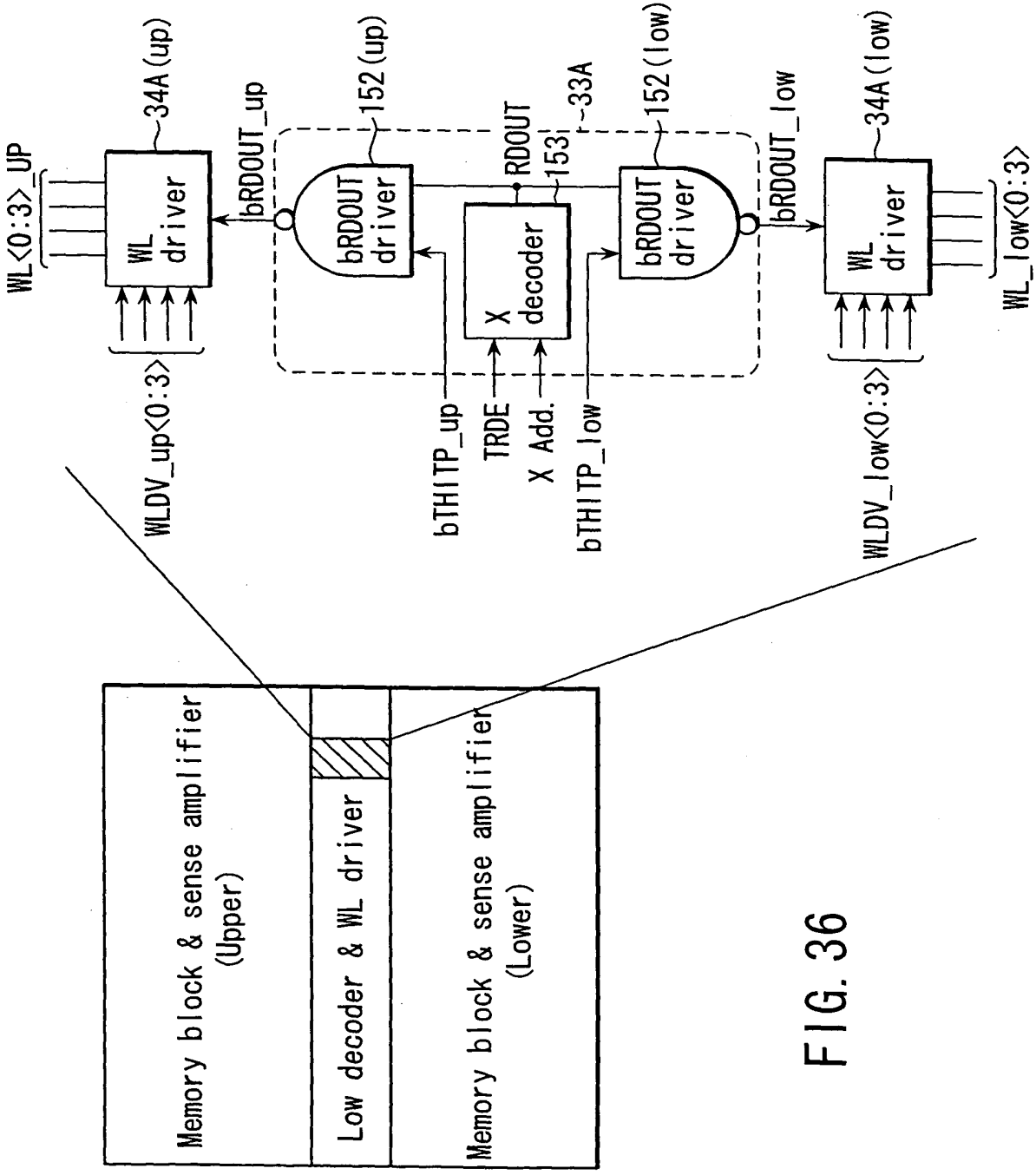

Memory block & sense amplifier (Upper)
Low decoder & WL driver
Memory block & sense amplifier (Lower)
WL<0:3>_UP
34A (up)
WL driver
WLDV_up<0:3>
bRDOUT_up
152 (up)
bRDOUT driver
bTHITP_up
RDOUT
153
X decoder
TRDE
X Add.
33A
152 (low)
bRDOUT driver
bTHITP_low
bRDOUT_low
34A (low)
WL driver
WLDV_low<0:3>
WL_low<0:3>

FIG. 36

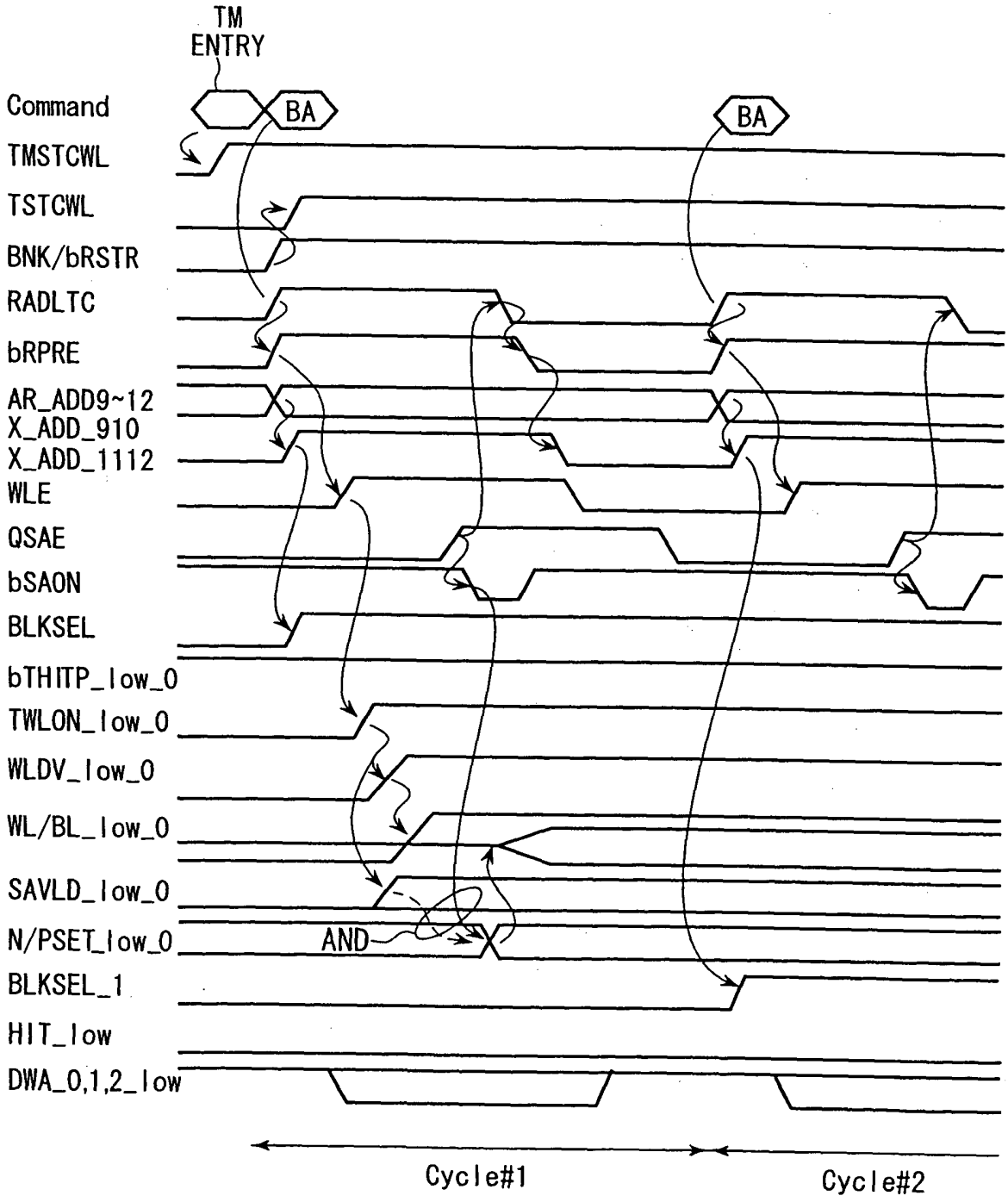

TM
ENTRY
Command
BA
BA
TMSTCWL
TSTCWL
BNK/bRSTR
RADLTC
bRPRE
AR_ADD9~12
X_ADD_910
X_ADD_1112
WLE
QSAE
bSAON
BLKSEL
bTHITP_low_0
TWLON_low_0
WLDV_low_0
WL/BL_low_0
SAVLD_low_0
N/PSET_low_0
AND
BLKSEL_1
HIT_low
DWA_0,1,2_low
Cycle#1
Cycle#2

FIG. 37

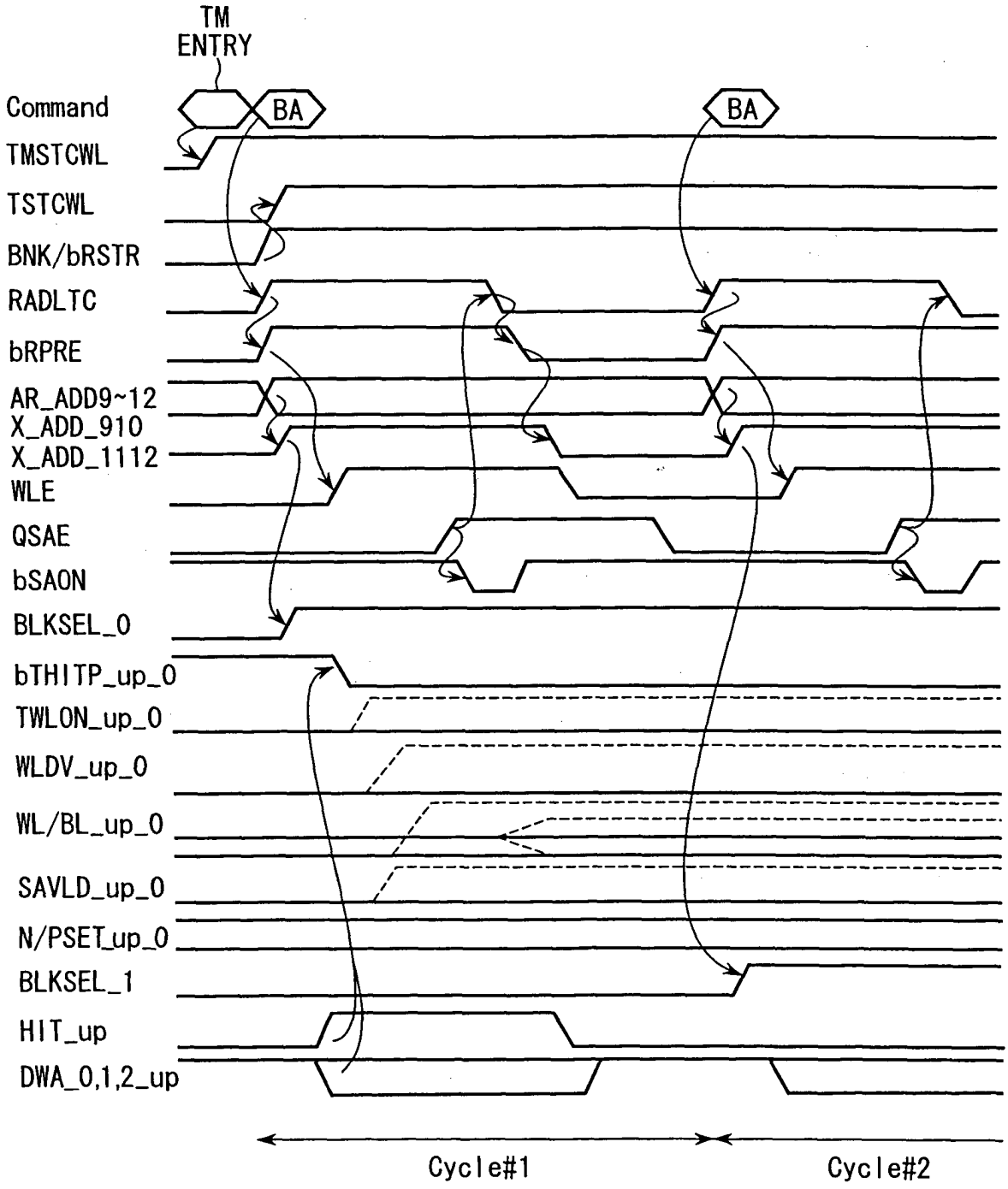

TM
ENTRY
Command
BA
BA
TMSTCWL
TSTCWL
BNK/bRSTR
RADLTC
bRPRE
AR_ADD9~12
X_ADD_910
X_ADD_1112
WLE
QSAE
bSAON
BLKSEL_0
bTHITP_up_0
TWLON_up_0
WLDV_up_0
WL/BL_up_0
SAVLD_up_0
N/PSET_up_0
BLKSEL_1
HIT_up
DWA_0,1,2_up
Cycle#1
Cycle#2

FIG. 38

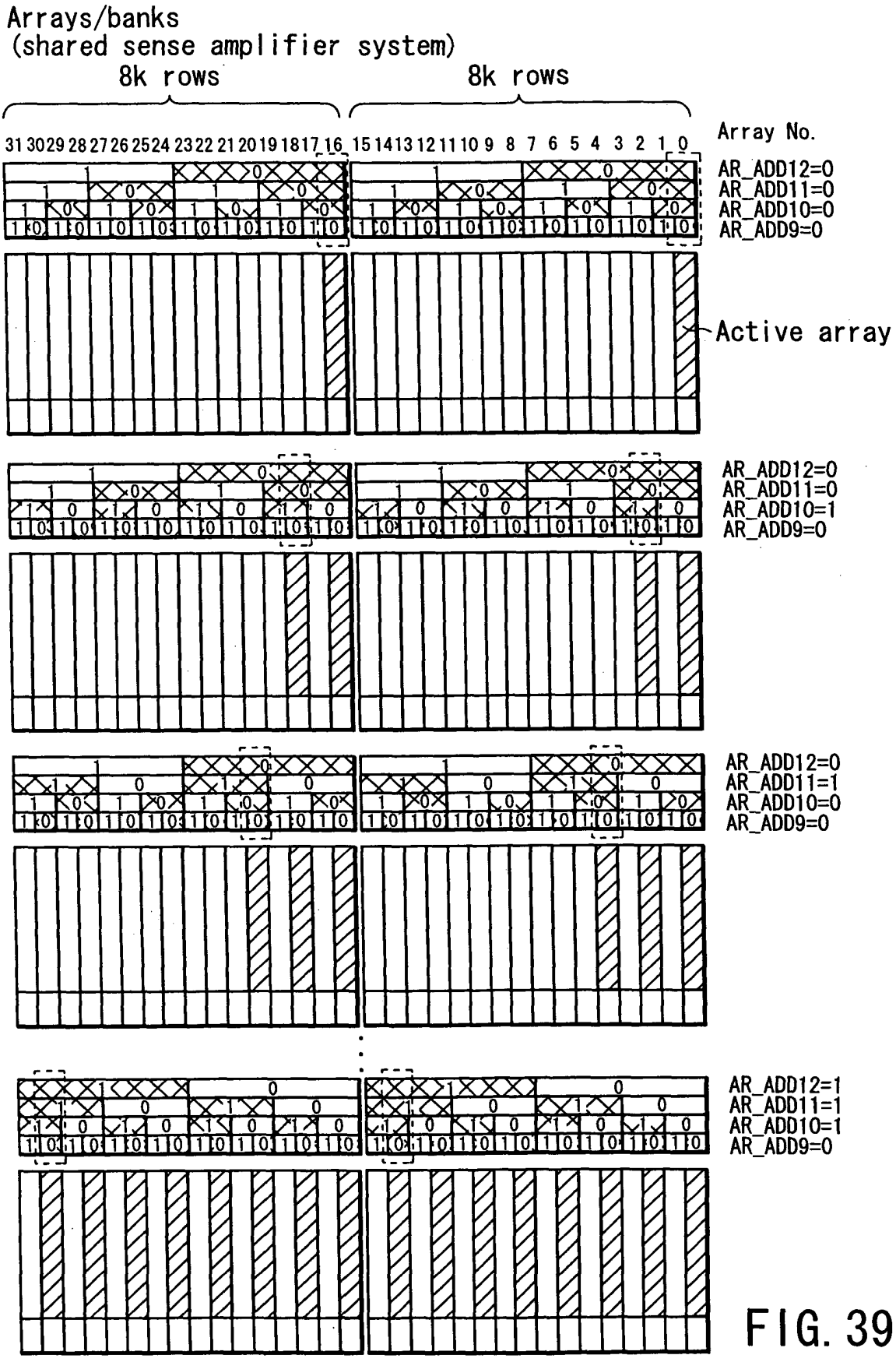

32 Arrays/banks
(shared sense amplifier system)
8k rows
8k rows
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Array No.
AR_ADD12=0
AR_ADD11=0
AR_ADD10=0
AR_ADD9=0
Active array
AR_ADD12=0
AR_ADD11=0
AR_ADD10=1
AR_ADD9=0
AR_ADD12=0
AR_ADD11=1
AR_ADD10=0
AR_ADD9=0
AR_ADD12=1
AR_ADD11=1
AR_ADD10=1
AR_ADD9=0

FIG. 39

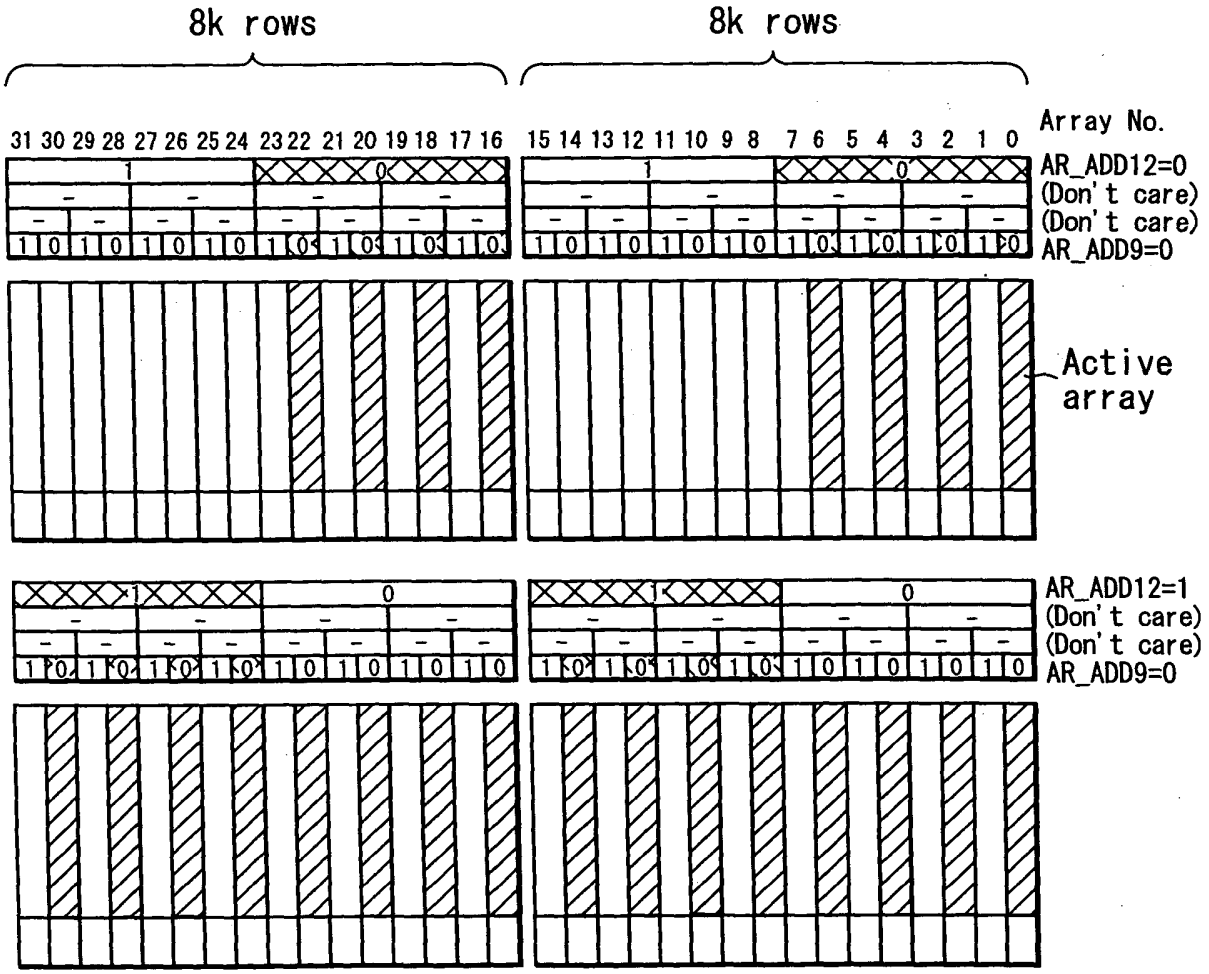

8k rows
8k rows
Array No.
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
AR_ADD12=0
(Don't care)
(Don't care)
AR_ADD9=0
Active array
AR_ADD12=1
(Don't care)
(Don't care)
AR_ADD9=0

FIG. 40

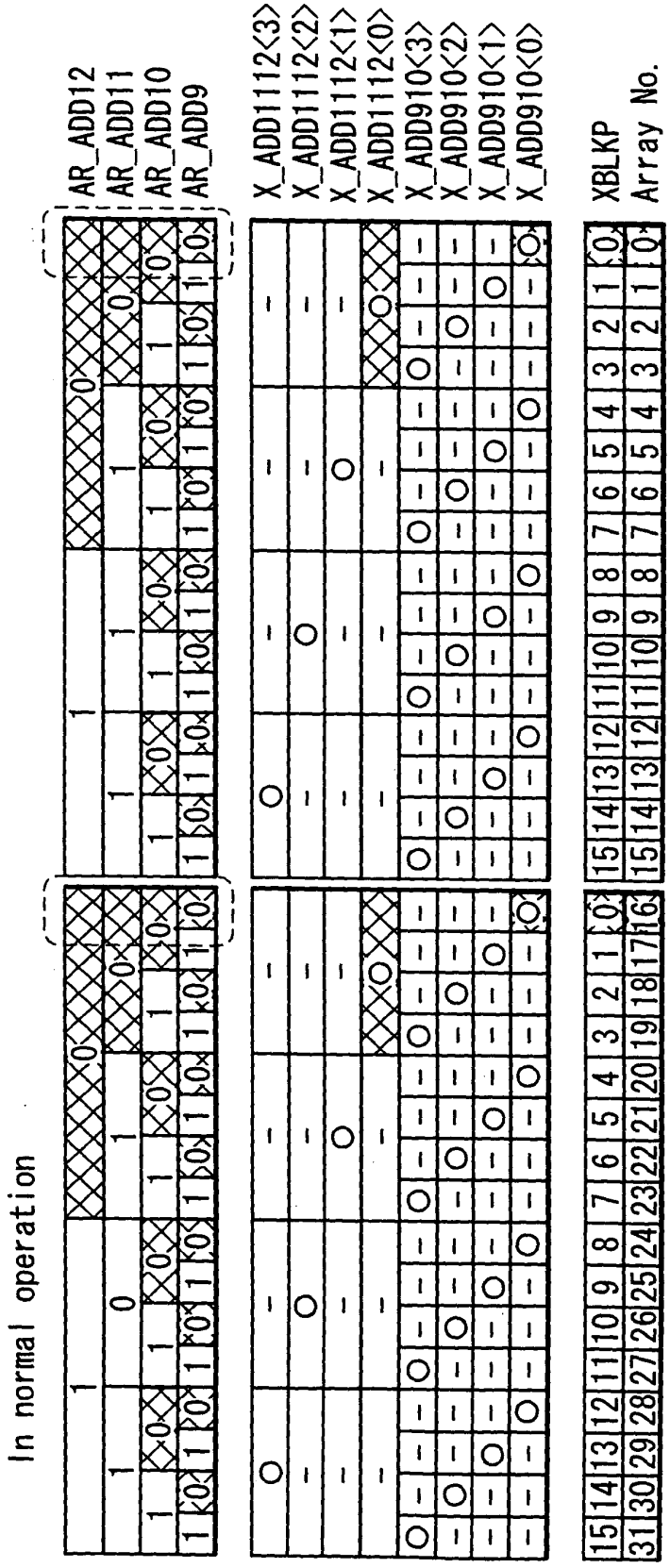

In normal operation
AR_ADD12
AR_ADD11
AR_ADD10
AR_ADD9
X_ADD1112<3>
X_ADD1112<2>
X_ADD1112<1>
X_ADD1112<0>
X_ADD910<3>
X_ADD910<2>
X_ADD910<1>
X_ADD910<0>
XBLKP
Array No.

FIG. 41A

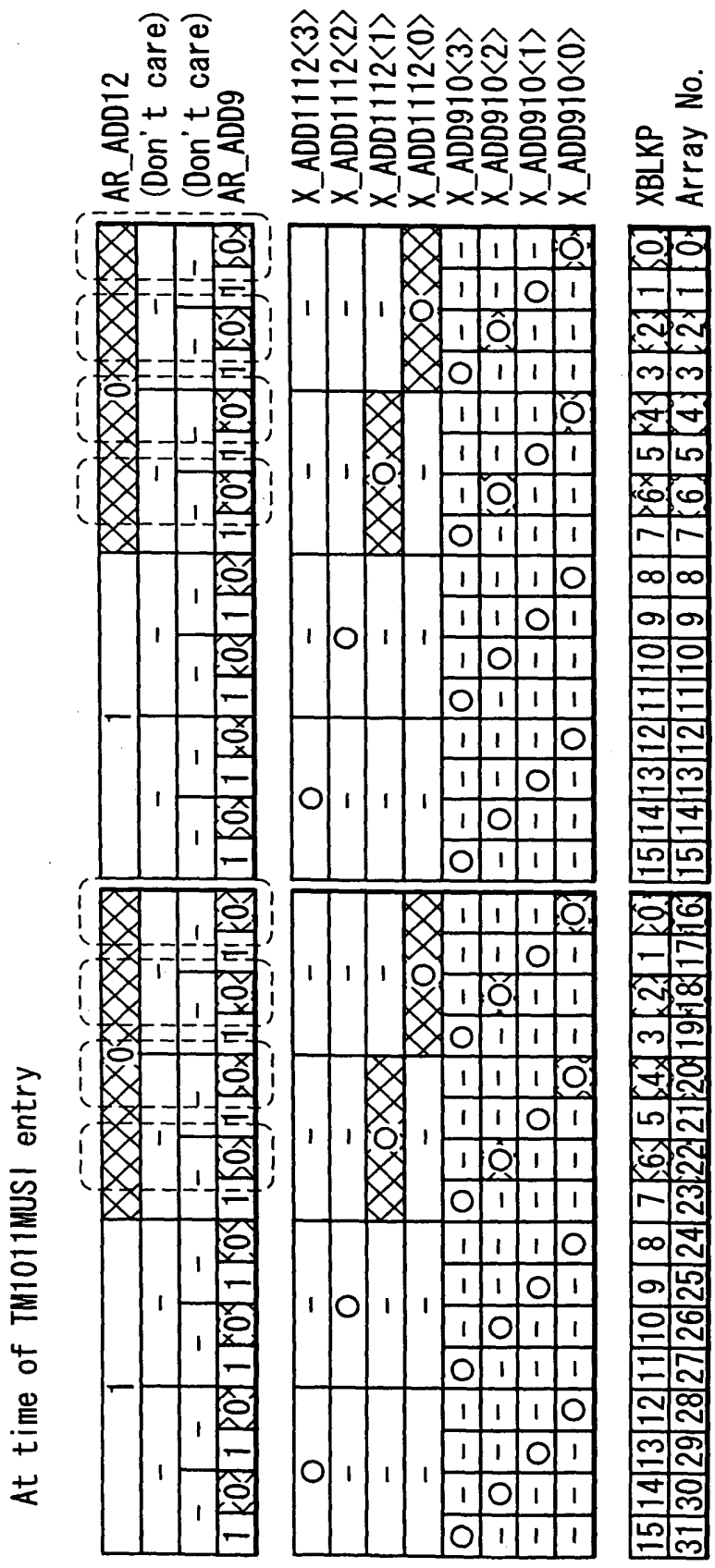

At time of TM1011MUSI entry
AR_ADD12
(Don't care)
(Don't care)
AR_ADD9
X_ADD1112<3>
X_ADD1112<2>
X_ADD1112<1>
X_ADD1112<0>
X_ADD910<3>
X_ADD910<2>
X_ADD910<1>
X_ADD910<0>
XBLKP
Array No.

FIG. 41B

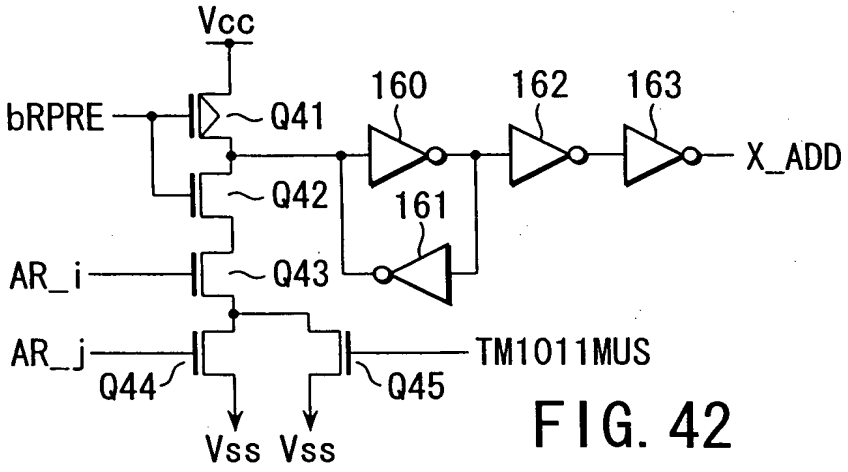
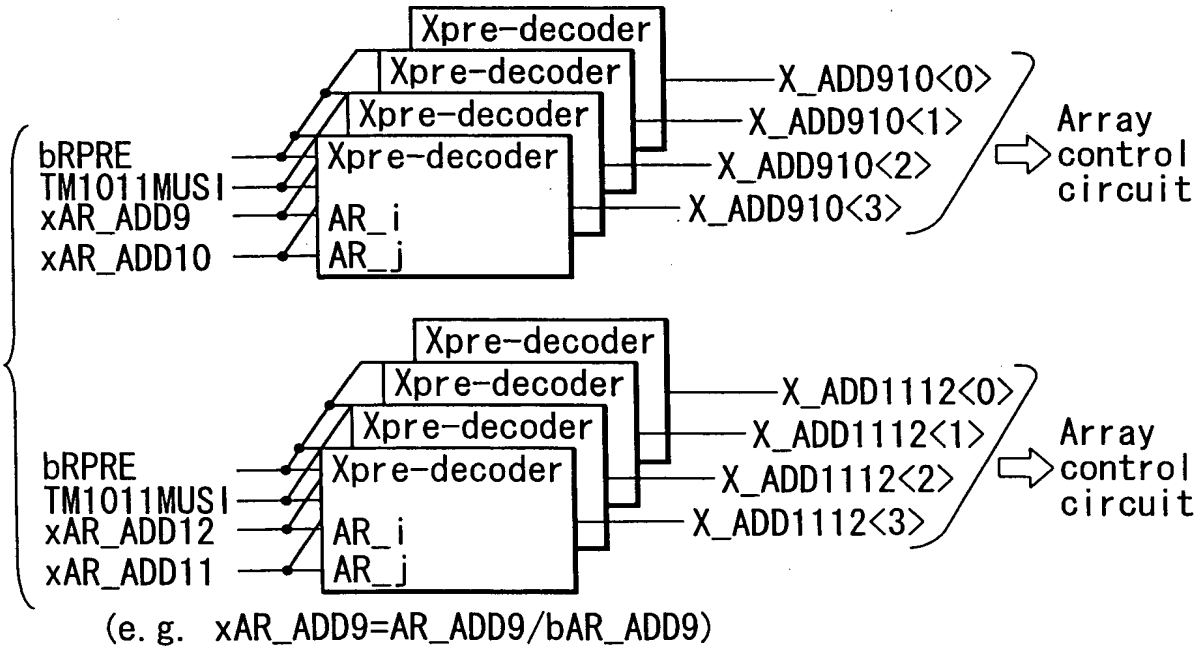


FIG. 42



(e.g. xAR_ADD9=AR_ADD9/bAR_ADD9)

FIG. 43

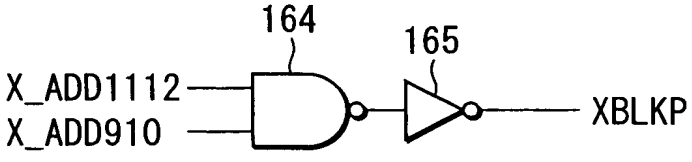


FIG. 44

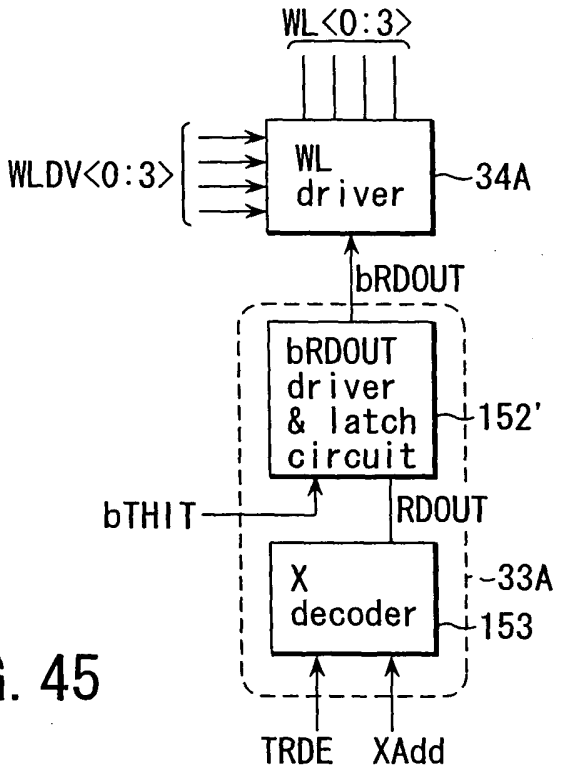


FIG. 45

TRDE control circuit

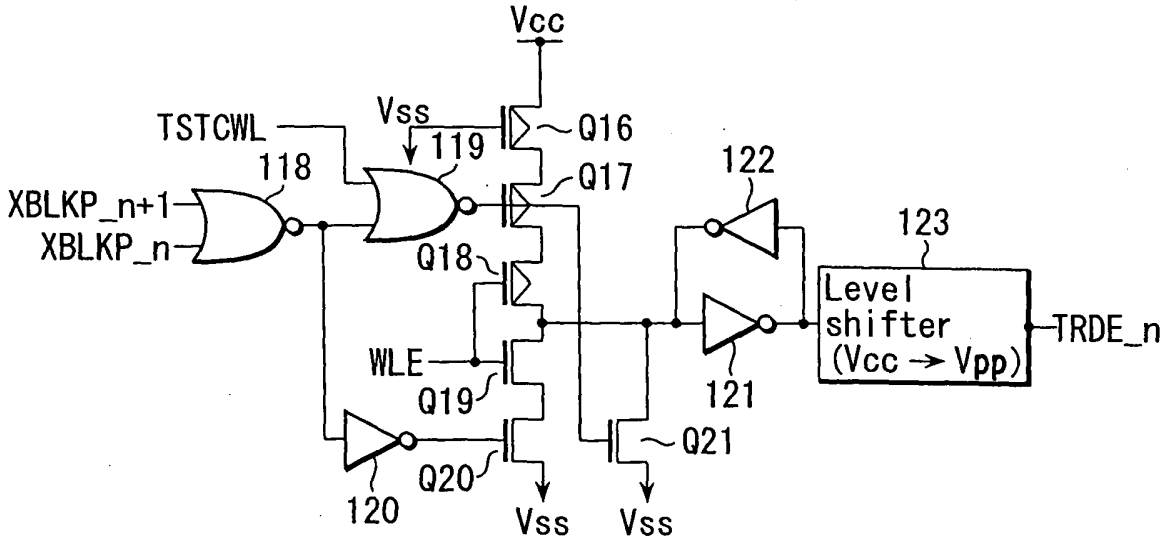


FIG. 46

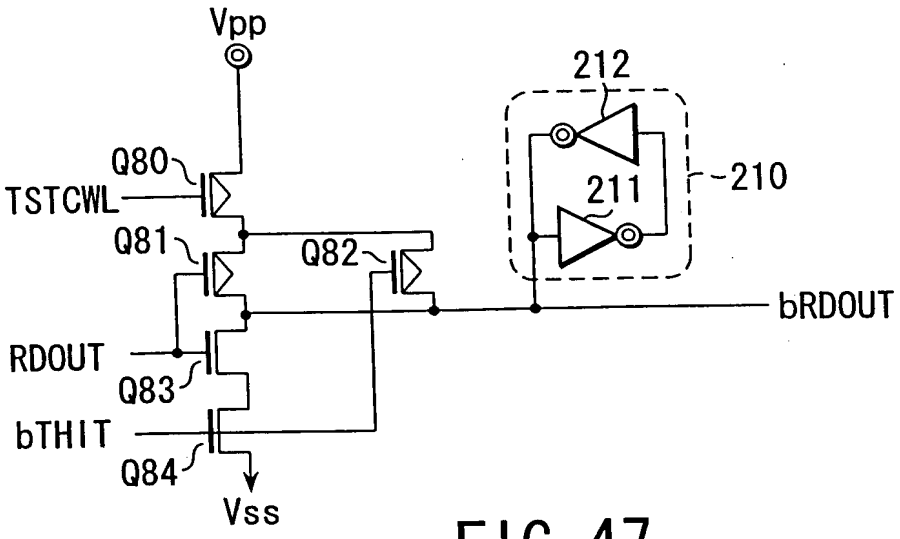

Vpp
212
Q80
TSTCWL
211
210
Q81
Q82
bRDOUT
RDOUT
Q83
bTHIT
Q84
Vss

FIG. 47

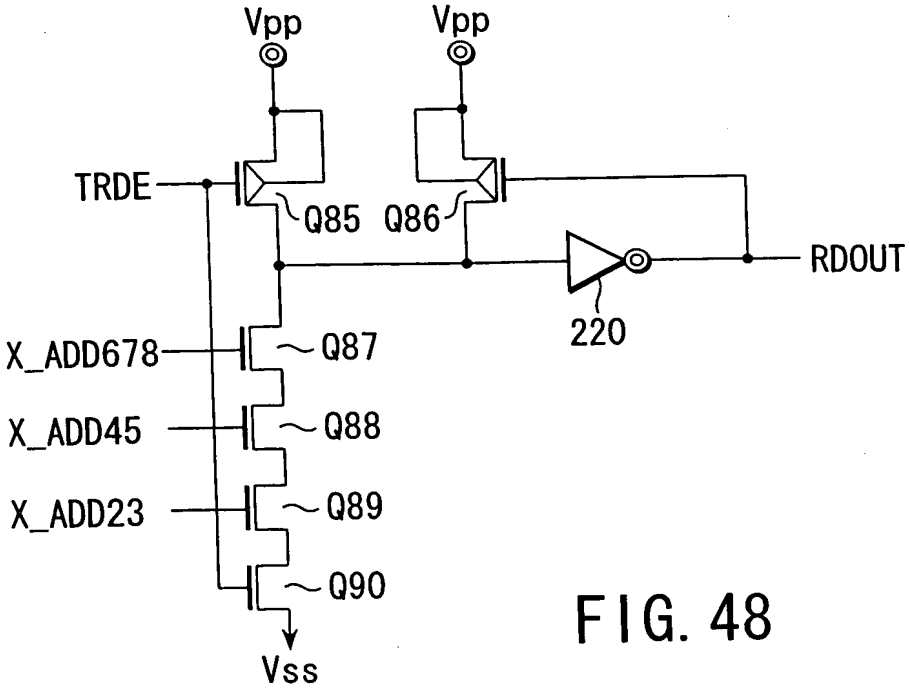

Vpp
Vpp
TRDE
Q85
Q86
RDOUT
220
X_ADD678
Q87
X_ADD45
Q88
X_ADD23
Q89
Q90
Vss

FIG. 48

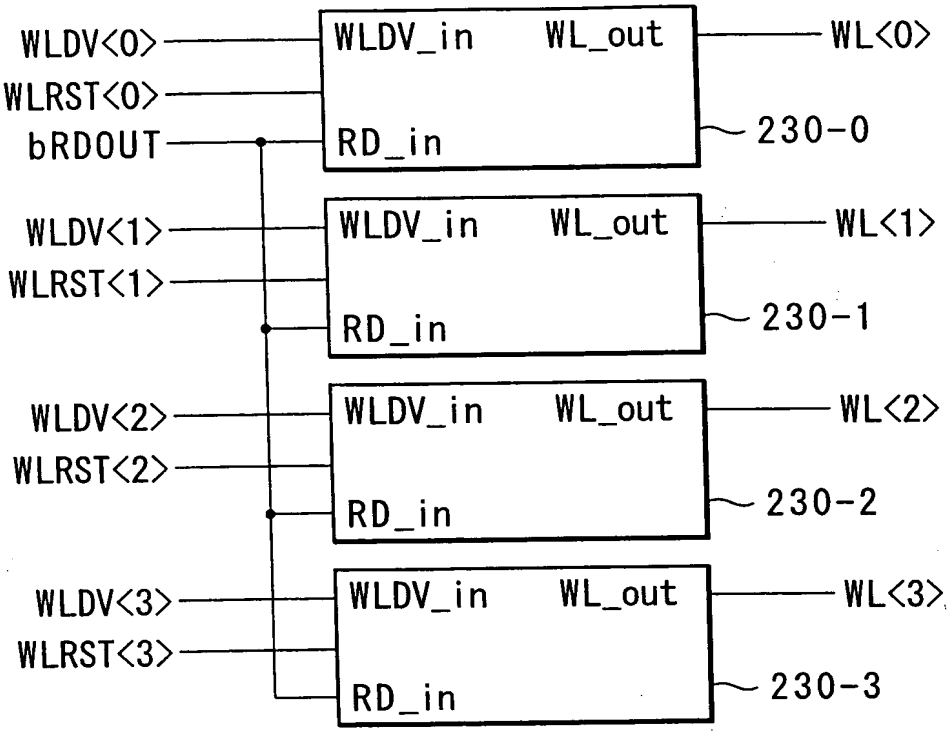

WLDV<0>
WLRST<0>
bRDOUT
WLDV_in
WL_out
RD_in
WL<0>
230-0
WLDV<1>
WLRST<1>
WLDV_in
WL_out
RD_in
WL<1>
230-1
WLDV<2>
WLRST<2>
WLDV_in
WL_out
RD_in
WL<2>
230-2
WLDV<3>
WLRST<3>
WLDV_in
WL_out
RD_in
WL<3>
230-3

FIG. 49

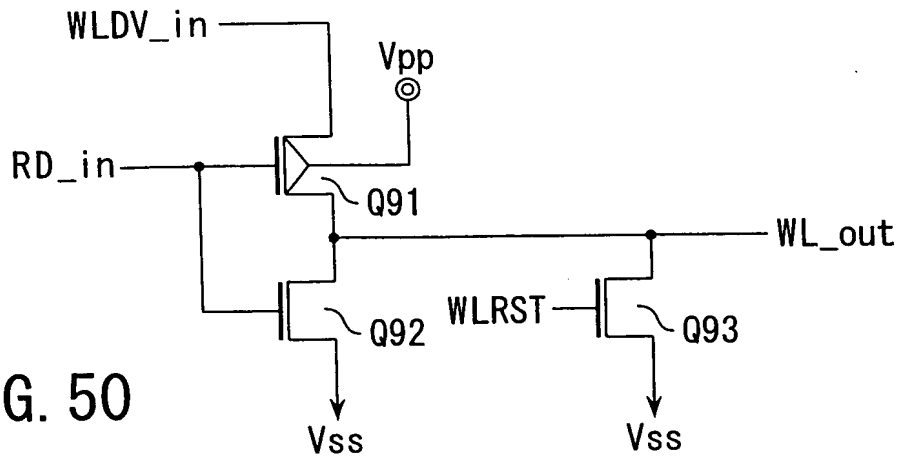

WLDV_in
Vpp
RD_in
Q91
WL_out
Q92
WLRST
Q93
Vss
Vss

FIG. 50

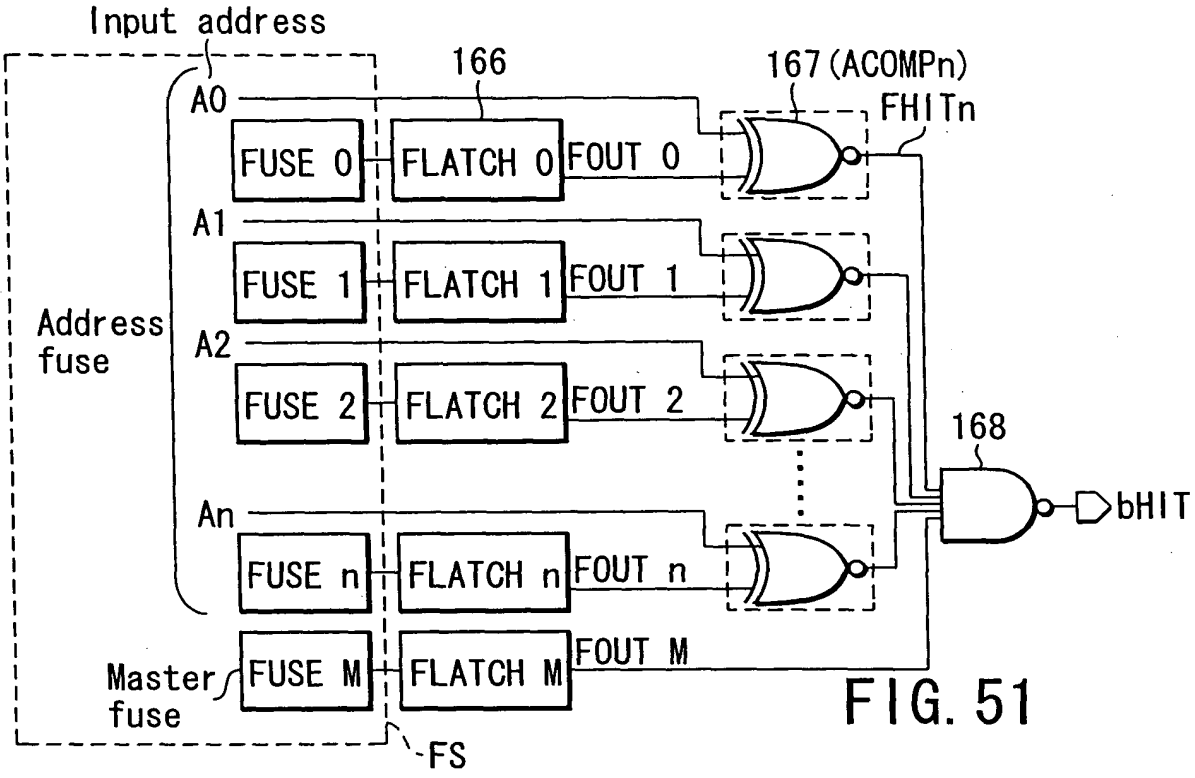


FIG. 51

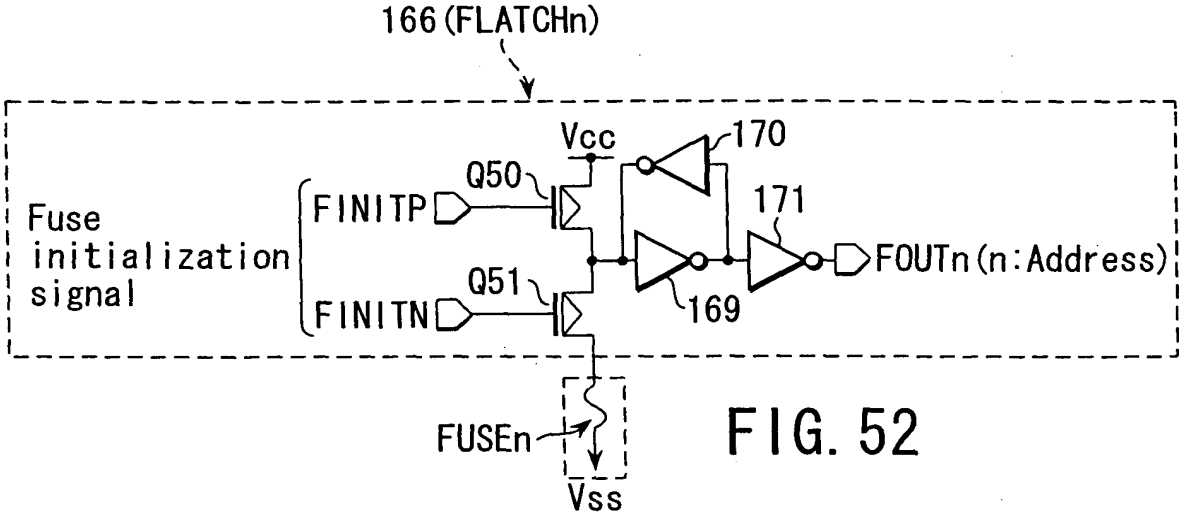


FIG. 52

FIG. 53

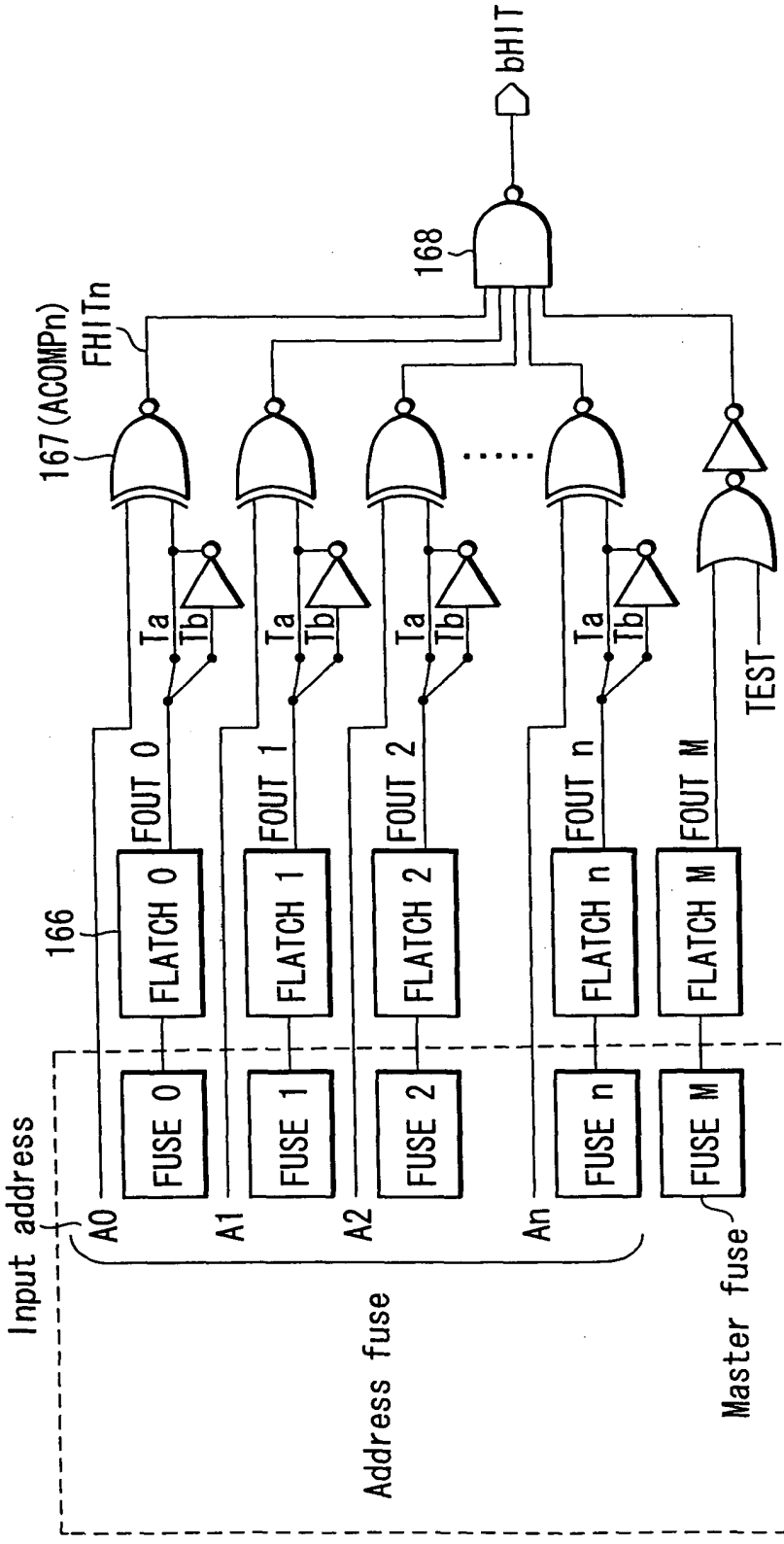

bHIT
168
167 (ACOMPn)
FHITn
Ta
Tb
TEST
FOUT 0
FOUT 1
FOUT 2
FOUT n
FOUT M
166
FLATCH 0
FLATCH 1
FLATCH 2
FLATCH n
FLATCH M
FS
FUSE 0
FUSE 1
FUSE 2
FUSE n
FUSE M
Input address
A0
A1
A2
An
Address fuse
Master fuse

FIG. 54

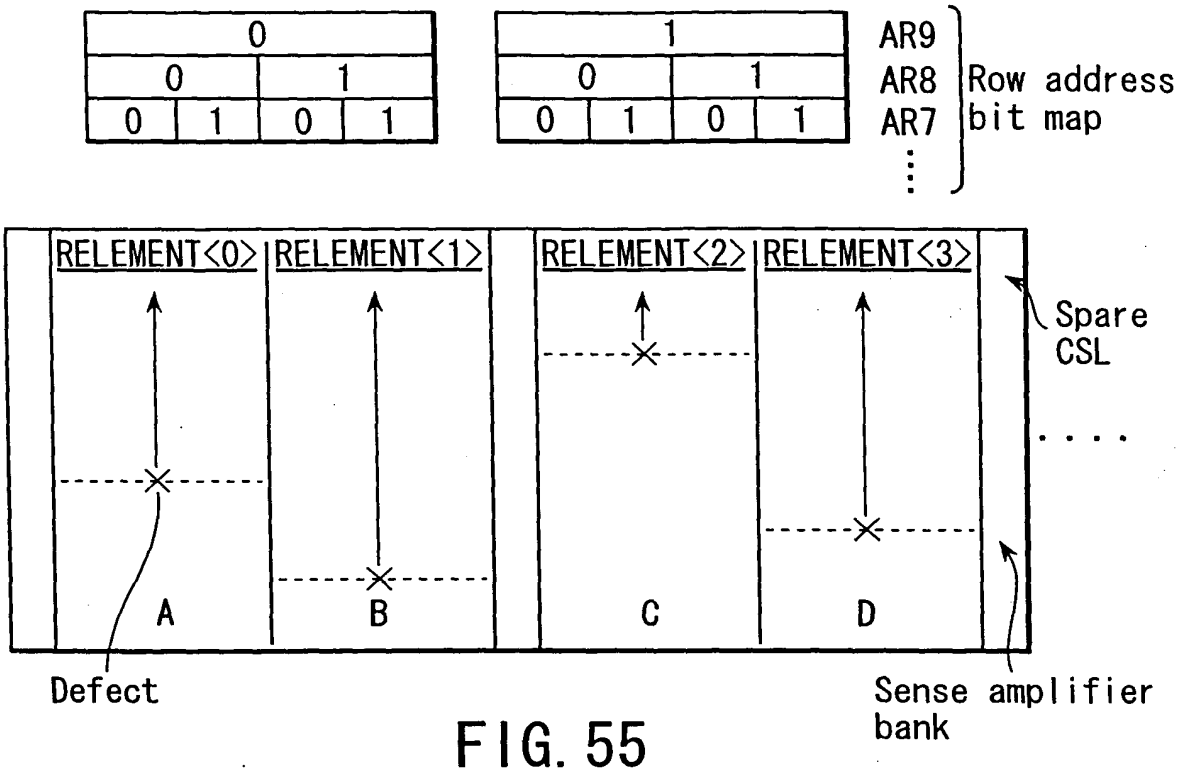

0
0
1
0
1
0
1
1
0
1
0
1
AR9
AR8
AR7
Row address bit map
RELEMENT<0>
RELEMENT<1>
RELEMENT<2>
RELEMENT<3>
Spare CSL
A
B
C
D
Defect
Sense amplifier bank

FIG. 55

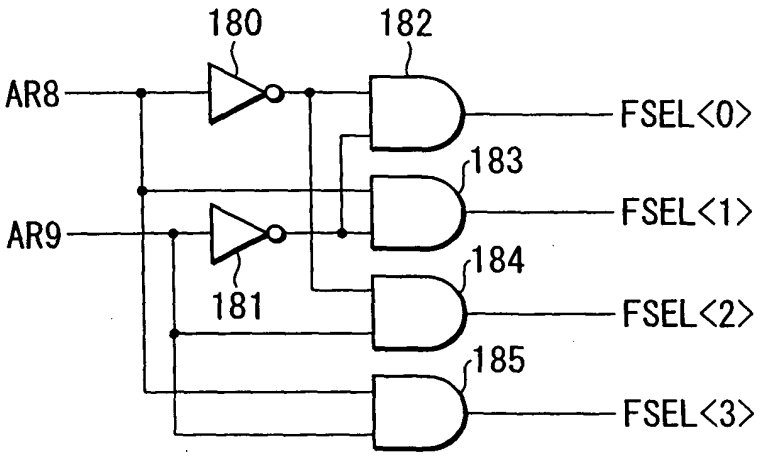

180
182
AR8
AR9
181
183
184
185
FSEL<0>
FSEL<1>
FSEL<2>
FSEL<3>

FIG. 56

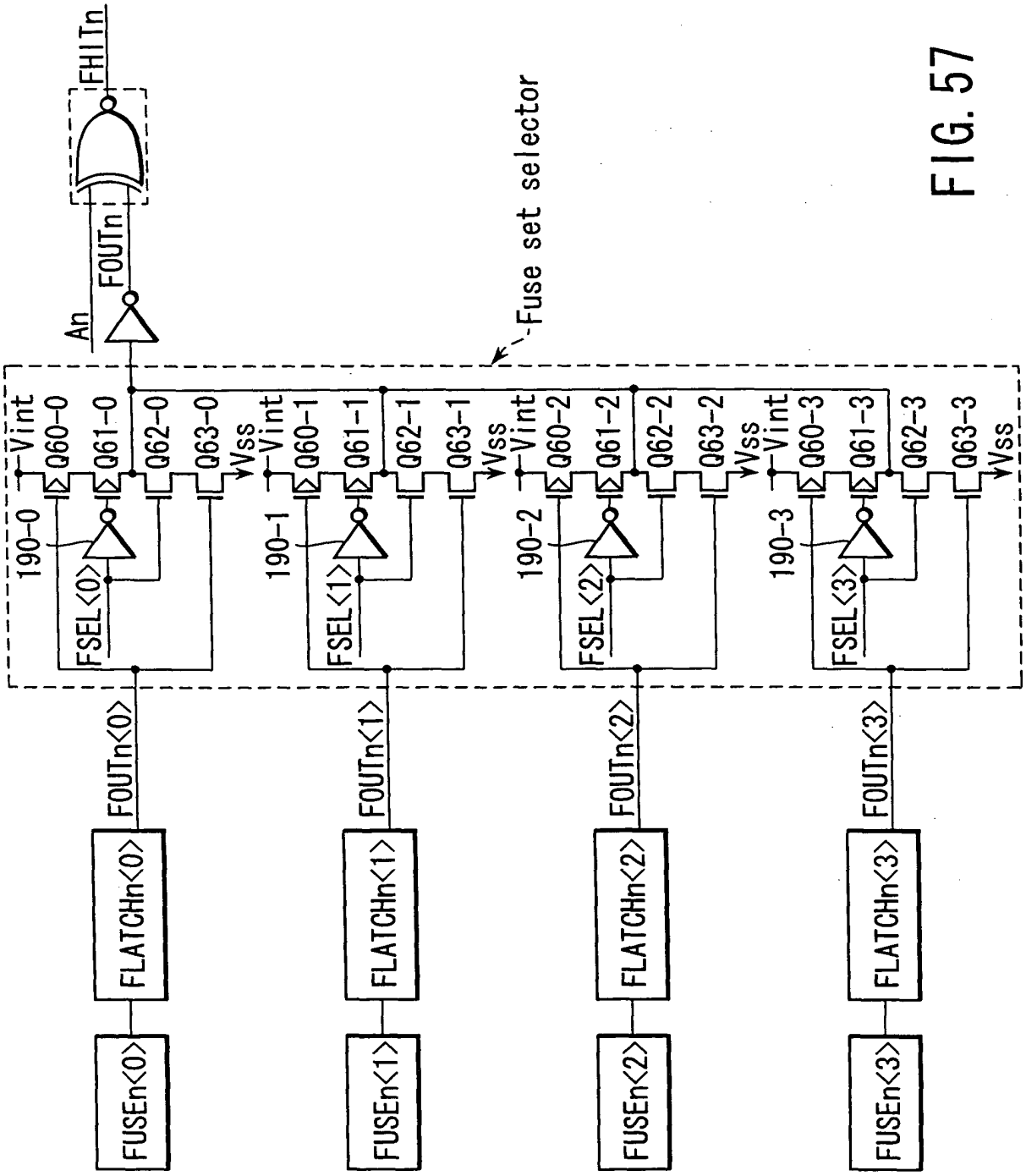

FHITn
An
FOUTn
Fuse set selector
Vint
Q60-0
Q61-0
Q62-0
Q63-0
Vss
Q60-1
Q61-1
Q62-1
Q63-1
Q60-2
Q61-2
Q62-2
Q63-2
Q60-3
Q61-3
Q62-3
Q63-3
190-0
190-1
190-2
190-3
FSEL<0>
FSEL<1>
FSEL<2>
FSEL<3>
FOUTn<0>
FOUTn<1>
FOUTn<2>
FOUTn<3>
FLATCHn<0>
FLATCHn<1>
FLATCHn<2>
FLATCHn<3>
FUSEn<0>
FUSEn<1>
FUSEn<2>
FUSEn<3>

FIG. 57

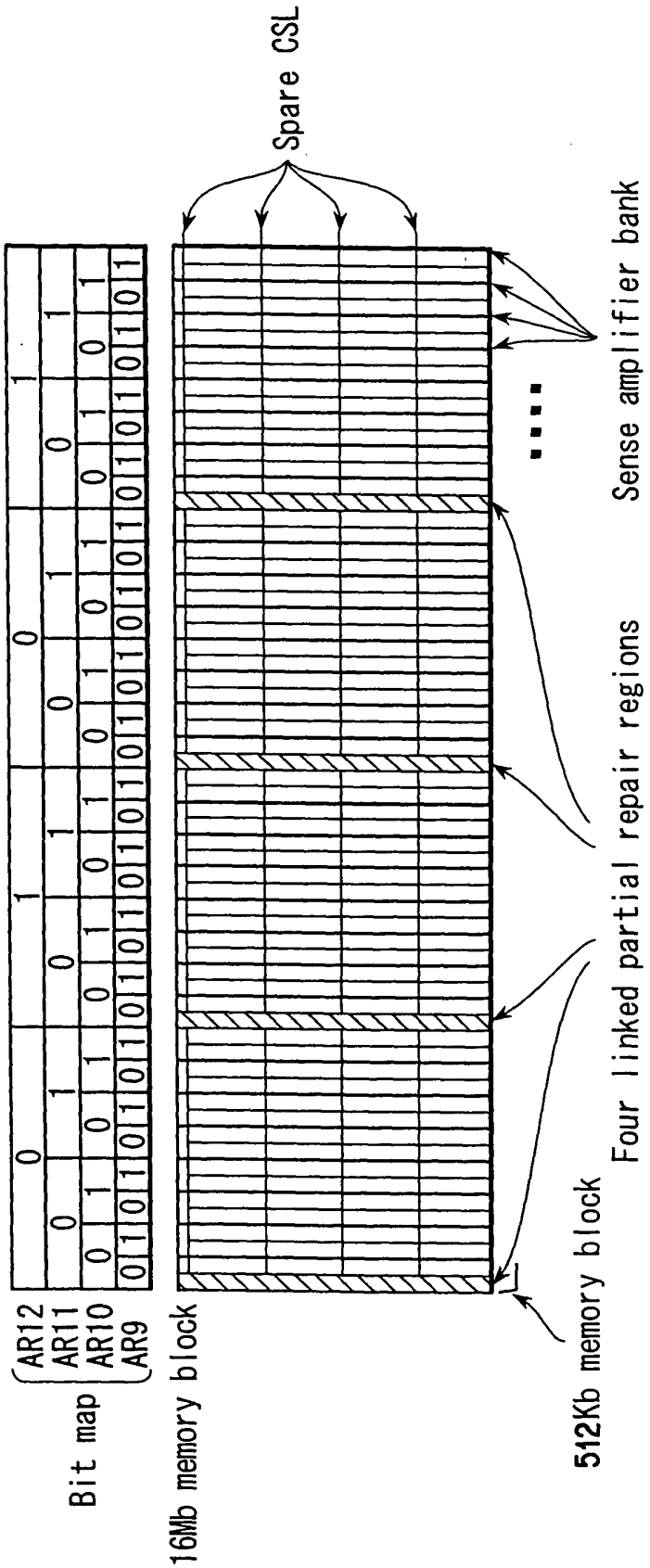

Spare CSL
Sense amplifier bank
Four linked partial repair regions
512Kb memory block
16Mb memory block
Bit map
AR12
AR11
AR10
AR9

FIG. 58

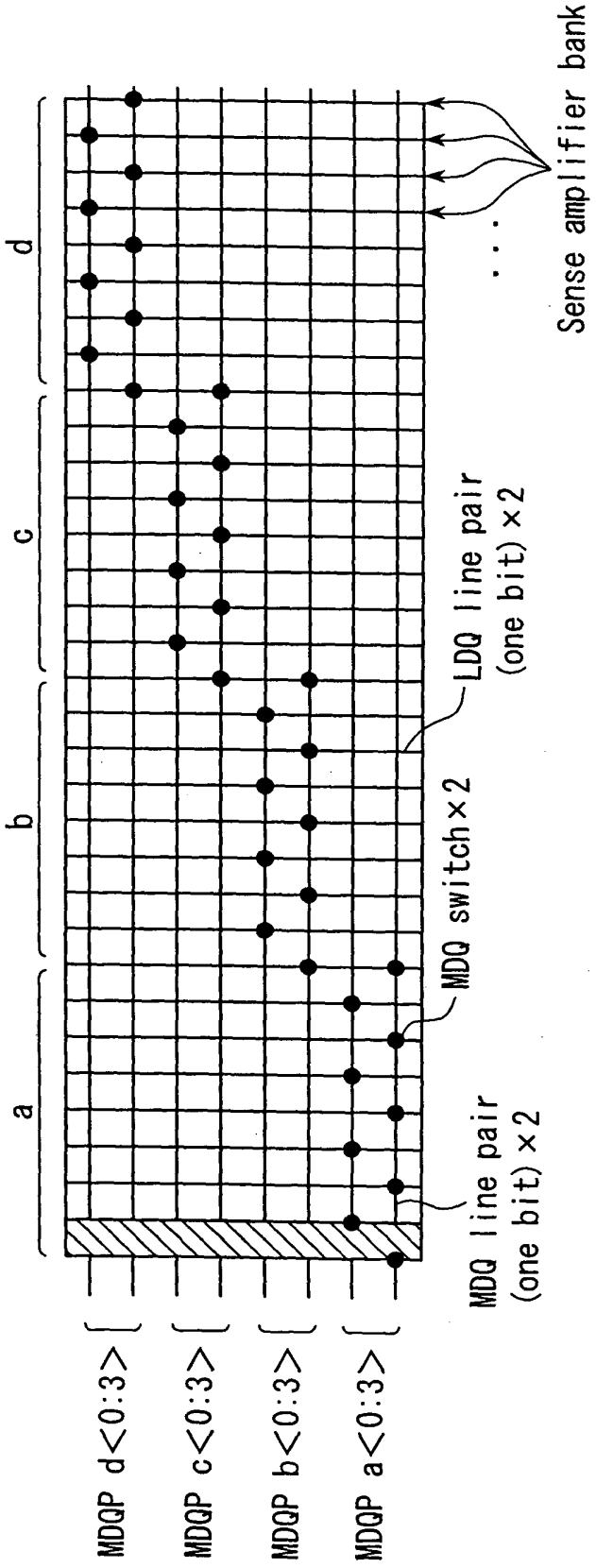

Sense amplifier bank
. . .
LDQ line pair
(one bit) ×2
MDQ switch×2
MDQ line pair
(one bit) ×2
a
b
c
d
MDQP d<0:3>
MDQP c<0:3>
MDQP b<0:3>
MDQP a<0:3>

FIG. 59

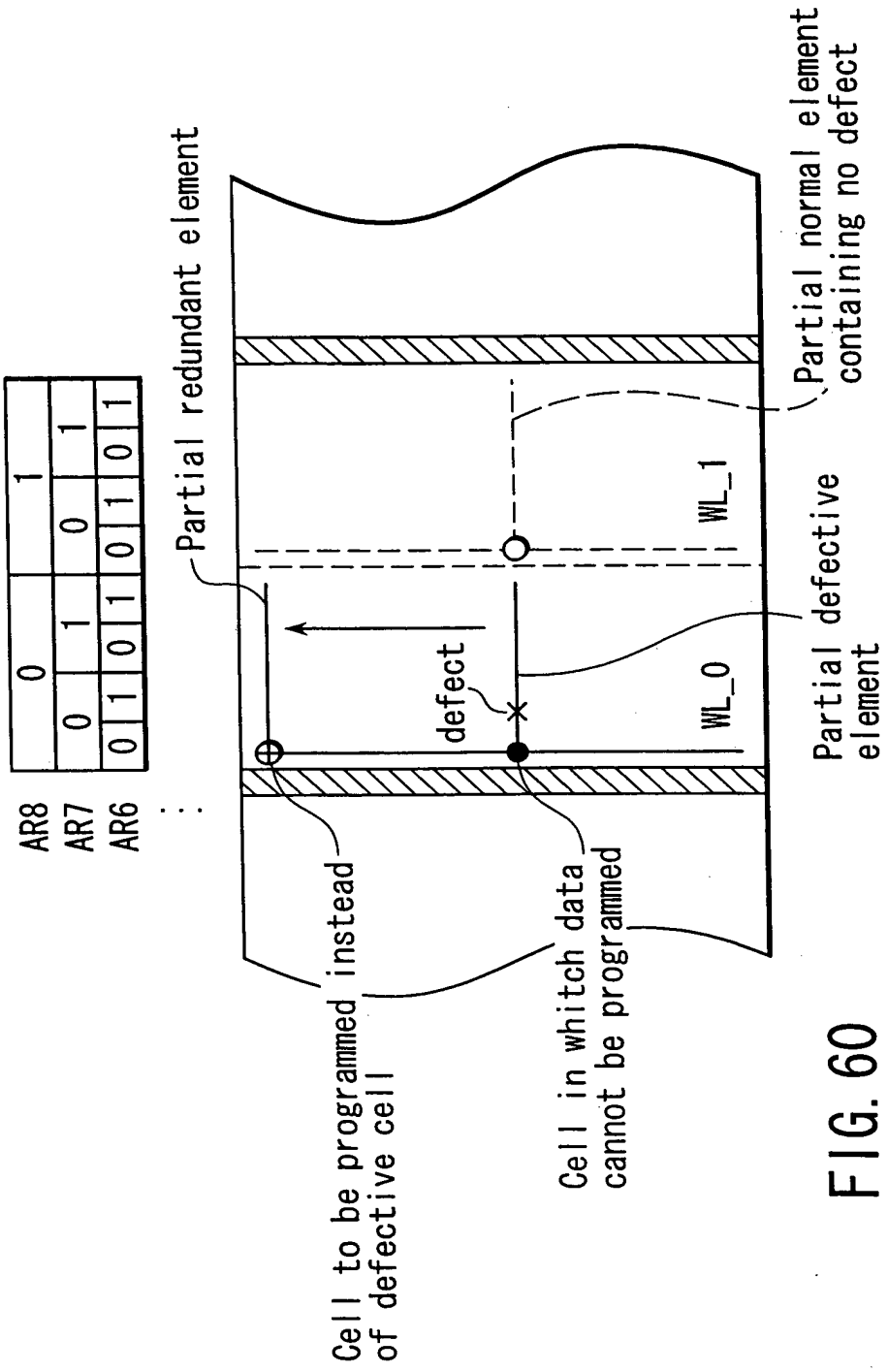

AR8
AR7
AR6
Partial redundant element
Partial normal element containing no defect
WL_1
WL_0
defect
Partial defective element
Cell to be programmed instead of defective cell
Cell in whitch data cannot be programmed

FIG. 60

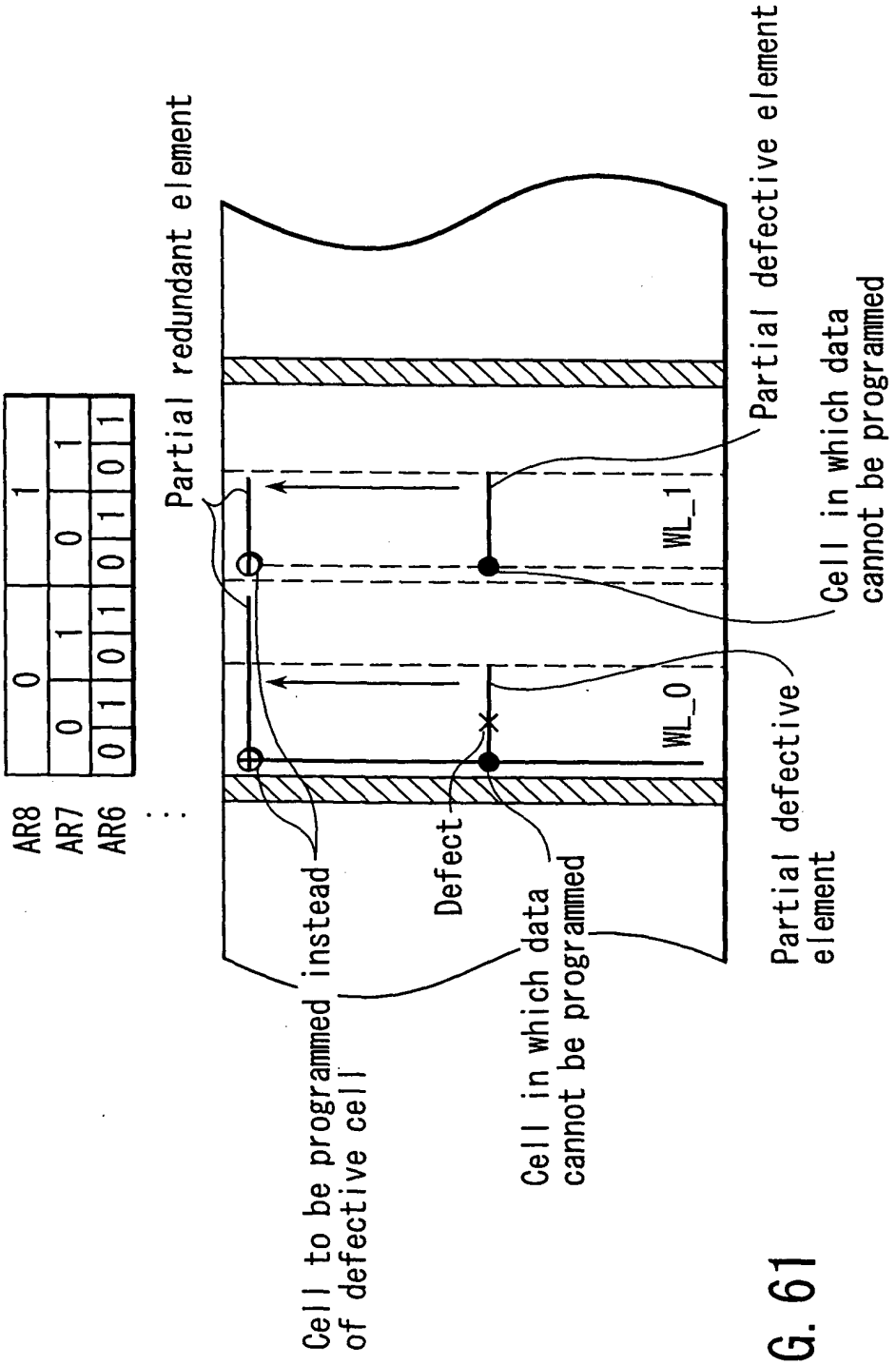

AR8
AR7
AR6
Partial redundant element
Partial defective element
Cell in which data cannot be programmed
WL_1
WL_0
Partial defective element
Defect
Cell in which data cannot be programmed
Cell to be programmed instead of defective cell

FIG. 61

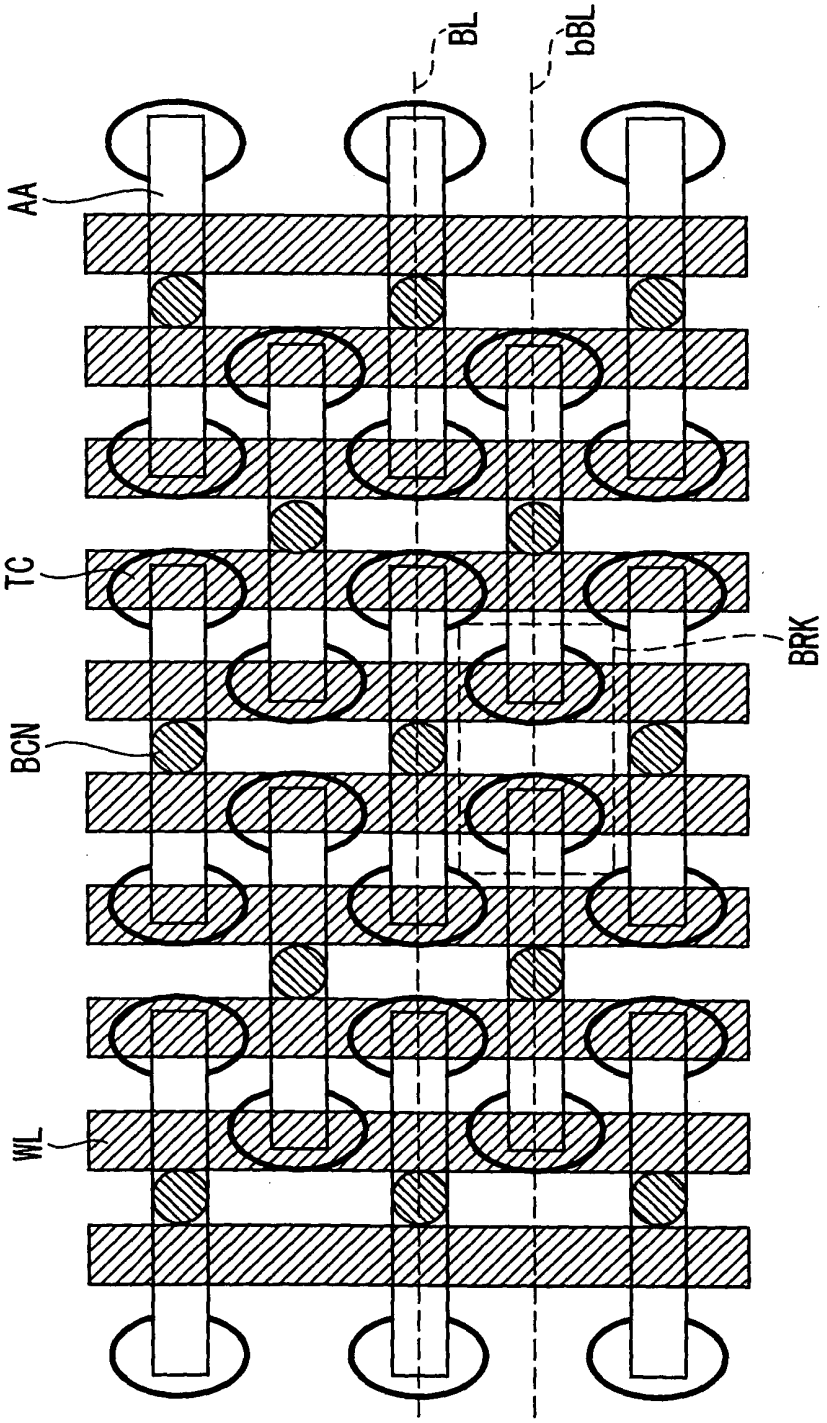


FIG. 62